PATRICIA S. LEE
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EDUCATION: ***University of California, Irvine (UCI)***
PhD Computer Science, 2013

COMPUTER SKILLS:
Languages: C, C++, C#.NET, Java, Perl, Python, T-SQL, Verilog, SystemVerilog/UVM, and e.
Protocols: PCIe, Serial Attached SCSI (SAS), Serial Advanced Technology Attachment (SATA)
Tools: Dini Group Xilinx Virtex™ 7 FPGA Development Board, Synopsys VCS, Cadence Incisive, PostgreSQL, mySQL, Visual Studio, Subversion, ClearCase/ClearQuest, VSS, Eclipse, .NET Framework
Operating Systems: Microsoft Windows, Unix/Linux, Mac OS, Apache Server

ACADEMIC EXPERIENCE:
Visiting PhD Scholar, UCI. (Jan. 2012 – Present)

- ***Visiting PhD Scholar:*** Research in natural language processing of specification for generation of assertions and in securing of cyber-physical systems. Research in hardware description languages (HDLs) and embedded systems at the behavioral level and RTL with an emphasis in security, formal verification, and simulation-based validation. Work with the VIS benchmarks to simulate within the Synopsys environment, verification of each design, and creation of several erroneous designs to compare simulation-based validation with model checking using the CTL (Computational Tree Logic) properties. Work with implementing a design of the IEEE 1500, I^2C, and SPI specifications to create a benchmark for testing automatic test generation and response checking techniques for simulation-based validation.
- ***Instructor of Record:*** (Summer Session 2016) Teach a class in C++ programming as a second language. Develop curriculum, prepare and enhance lectures, create homework assignments, quizzes, midterm, final exams with solutions. Applied teaching methodologies to enable success for students. 1:1 student guidance and advising in office hours and via email. Negotiated and perform administrative duties. Manage one teaching assistant with approximately 50 students. Clarified appropriate rubric. (Summer Session 2012) Teach and lecture a class in computer systems architecture. Develop curriculum, create homework assignments, quizzes, midterm and final exams with solutions. Manage one teaching assistant with over 50 students.

Adjunct Professor, California State University Fullerton. (Aug. 2015 – Present)

- ***Instructor of Record***: (Fall Semester 2016) Develop curricula for online Python Certification Program. Create recorded lectures, online lab assignments, online exam materials. Advise students in one-on-one online office hours. Facilitate and structure online message boards, gradebooks, calendar, website, gradebooks. Coordinate with program managers and technical staff. (Spring Semester 2016) Operating systems and video game design classes. Create curricula for class homework assignments, quizzes, labs, and exams. 1:1 student guidance and advising in office hours and applied teaching methodologies to enable student success. (Fall Semester 2015) Four classes in C++ programming and a class in Python advanced programming. Over 150 students.

Adjunct Professor, Orange Coast College. (Jan. 2014 – Jun. 2014)

- ***Instructor of Record***: Facilitated labs and lectures for a class in C#.NET programming. Enhance and define curricula for class homework assignments, quizzes, labs, and exams. Structure class website gradebooks, dropboxes, messageboards, calendar. Over 40 students.

INDUSTRY EXPERIENCE:

Senior Engineer, Qualcomm. (Mar. 2014 – May 2015)

- ***QCT Digital Design - Modem***: Enhance test automation by leveraging SystemVerilog, SystemC, and UVM technology that resulted in 100% code coverage that significantly improved the quality of the digital modem chip. Standardize assembly tests and executable test plan (ETP) to automate SystemVerilog verification of vector unit (VU) instruction set. Automation scripts improve time to create testbenches, verify legacy features, ensure new features did not break current build. Several major timing issues uncovered by automated tests and consequently resolved by appropriate groups. Design, verification, and microkernel product features investigated, debugged in collaboration with analog, communications, and verification groups in narrowband TX/RX engine in symbol processor, VU, and integer unit blocks. Receive/provide feedback in design and code reviews for development and verification.

Principal Electronic Hardware Design/Firmware Engineer, Western Digital. (Jul. 2008 – Mar. 2013)

- ***Principal Electronic Hardware Design Engineer:*** Member of the System on a Chip (SoC) hardware design and verification team. Define, standardize, adapt SATA, SAS, PCIe block verification. Advocate, explain, guide transition of methodology from disparate technologies into one main technology.
- ***Principal Firmware Engineer:*** Member of the SoC Bring-up and Advanced Controller Firmware Teams as firmware engineer. Major contributions in successful bring-up of 3 programs. Coordinate with Functional Integrity Testing labs and uncover/assist in debugging of features/issues on prototype drives. Firmware development and field programmable gate array (FPGA) debugging with focus on SATA host interface. Receive/provide feedback in design and code reviews cross functionally across hardware/firmware groups in various functional units (SAS, SATA, Physical Interface, Testing, Architectures). Firmware compilation, testing, debugging and development for SAS. Full Disk Encryption (FDE) security system development and analysis. Central processing unit (CPU) benchmarking, performance analysis and reporting. Member of the Enterprise Systems Group as a system engineer. Failure analysis (FA) of drives regarding signal integrity, firmware, driver issues, operating system issues, protocol violation, various other areas of possible failure. Member of the Platform Engineering group as a firmware engineer. Resolve, convey or allocate resource to first-level FA issues, new feature development, system integration, vendor-specific support.

System Software Engineering Co-op, Unisys. (Jul. 2005 – Jul. 2008)

- Member of the development team. Extend open source project enhancing PostgreSQL with Unisys proprietary addition. Develop and implement system to port code to mainframe hardware system, feature upgrades, and support of a Java client interface to a mainframe database application enabling company with solution to maintain relations with customers on legacy networked databases running on legacy systems wanting to move into newer relational database systems on system agnostic hardware. Application updates, bug fixes, and testing. Contribute to meetings in receiving/providing feedback in code reviews, presentations and documentation.

AWARDS:

- ACM Richard Tapia Celebration of Diversity in Computing new faculty scholarship (2016)
- Women's Empowerment Initiative and the Academic and Professional Women of the University of California Irvine invited speaker (2016)
- VLSI Test Symposium (VTS) conference publication presentation (2012)
- Computing Research Association Committee on the Status of Women in Computing Research and Coalition to Diversify Computing (CRA-W/CDC) scholarship to attend the Computer Architecture Summer School at Northwestern University in Evanston, IL (2012)
- Microprocessor, Test and Verification (MTV) conference scholarship (2010)
- Achievement Rewards for College Scientists (ARCS) fellowship (Sep. 2008 – Jun. 2010)