

From the EIC



Sustaining an industry obsession

■ **DEVICE SCALING** has long been an accepted mantra, even an obsession, in the semiconductor industry, and if recent predictions are true, the march of deep-submicron (DSM) devices into the nanoscale era will continue. Process and device engineers will somehow find a way to overcome the looming technical challenges, just like they always have from the earliest MOS technology days. Long-range planning, such as that reflected in the *International Technology Roadmap for Semiconductors*, has only accelerated this trend. However, device scaling has a fundamental business purpose: either a cost advantage or a performance—and, therefore, price—advantage. At some point, the migration of process technology nodes becomes a return on investment (ROI) issue with direct consequences for the rest of the microelectronics industry. For design and test engineers, application developers, and system builders, maintaining the historic ROI for the semiconductor industry often means doing more with less.

Whether you see them as a technical obsession or a business necessity, DSM process technologies are here to stay, and scaling will continue for the foreseeable future. Design and test professionals must find ways to handle the challenges. They must also use the cost-performance opportunities presented by these process advances to build better, more reliable microelectronic systems. In this issue, guest editors Jaume Segura and Peter Maxwell have organized a special issue on defect-oriented testing in the DSM era that explores advances to meet test challenges posed by the coming generations of DSM technologies.

A highlight of this issue is a special section dedicated to the upcoming International Test

Conference. ITC Test Week is the flagship event of the test community. *D&T's* relationship with ITC, and with the test community in general, goes back many years. Every year, the ITC program chair helps choose the theme of this special section and serves as a guest editor for the presentation in *D&T*. Following this tradition, guest editors Rob Aitken and Don Wheeler have selected four articles representing the ITC theme of “stressing the fundamentals.” On behalf of *D&T*, I thank the ITC organizers, and the larger test community organized under the umbrella of the Test Technology Technical Council, for their continual support. We are proud to regularly publish a newsletter from TTTC.

Also in this issue, Marcello Dalpasso and his colleagues present a virtual, distributed-design modeling simulation and validation environment, JavaCAD, which can improve design productivity—another challenge posed by the growing complexity of systems on chips.

Finally, I am grateful to Gordon Roberts for his lengthy service to *D&T* in various capacities, including his recent service as area editor. Beginning this issue, Michel Renovell will serve as area editor for analog and mixed-signal test, in place of Gordon. Michel heads the Microelectronics Department of LIRMM (the Laboratoire d'Informatique, Robotique et Microélectronique de Montpellier). Welcome aboard. Michel!

A handwritten signature in cursive script that reads "Rajesh Gupta".

Rajesh Gupta
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IEEE Design & Test of Computers