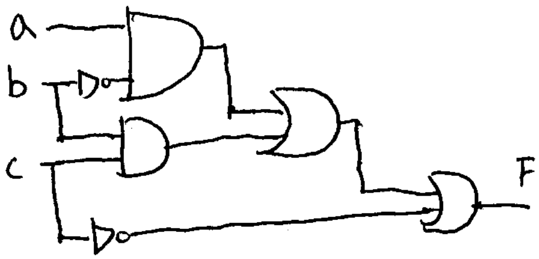
2.9 (a) OR (b) AND (c) NOT

2.11 (a) c = 1 ∴ 1 (d) d = 1 ∴ 1

2.13 (b) a = 0 ∴ 0 (c) b. c. d = 0 ∴ 0

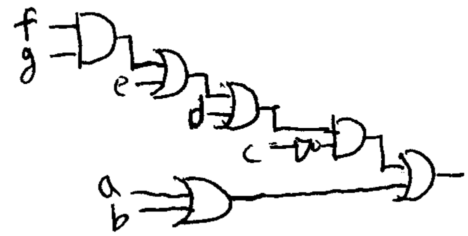
2.16

(a)

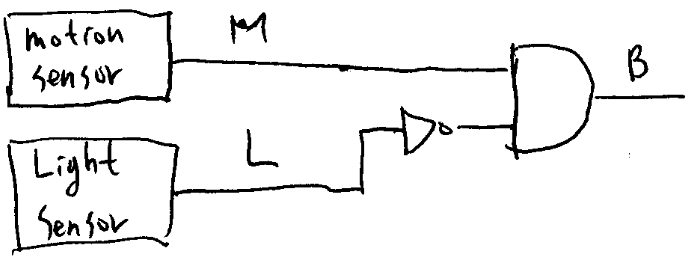


2.18

(c)



2.19



2.21

$F = M + M'L$

2.24

(a) $T \cdot H' + T'H$ (b) $(H' T + T' H)' = (T'+H)(T+H') = TH + T'H'$

2.27

$a'bc + a'bd' + ab' + ac + abc + adc$ = a'bc + a'bd + ab' + ac

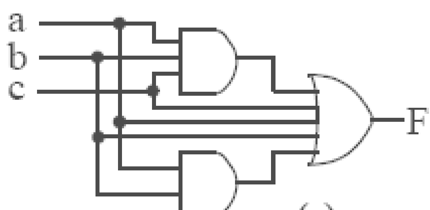
2.29

$(ac' + abd' + acd)' = (a'+c)(a'+b'+d)(a'+c'+d')$

= a' + c(b'+d)(c'+d')
= a' + (cb' + cd)(c'+d')
= a' + (cb'c' + cb'd' + cdc' + cdd')
= a' + cb'd'

2.30.c.

F(a,b,c) = abc + ab + a + b + c



(c)

2.31

F = (ab' + b)'

2.34.c

Inputs Outputs

a	b	c	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

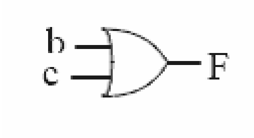
2.36

F = a'b'c + a'bc' + a'bc + ab'c + abc' + abc

2.37

F = a'b'c + a'bc' + a'bc + ab'c + abc' + abc
F = a'(b'c + bc' + bc) + a(b'c + bc' + bc)
F = a'(b'c + b(c' + c)) + a(b'c + b(c' + c))
F = a'(b'c + b) + a(b'c + b)
F = (a' + a)(b'c + b)
F = b'c + b
F = (b'+b)(c+b)
F = (c+b)

2.44



2.47(a)

F(a,b,c) = a’bc + abc’ + abc

2.50

The circuit in Figure 2.4 represents the equation H = ab + b’c. In canonical sum-of-minterms form, H = abc’ + abc + a’b’c + ab’c, which is equivalent to G.

2.54

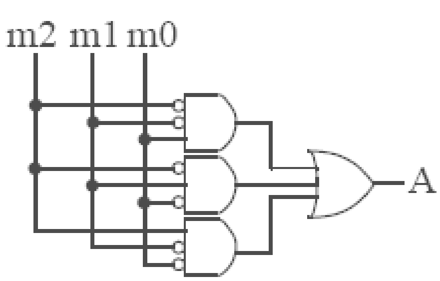
Step 1 - Capture the function

Inputs			Outputs
m2	m1	m0	A
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Step 2 - Convert to equations

A = m2’m1’m0 + m2’m1m0’ + m2m1’m0’

Step 3 - Implement as a gate-based circuit



2.57

Step 1 - Capture the function

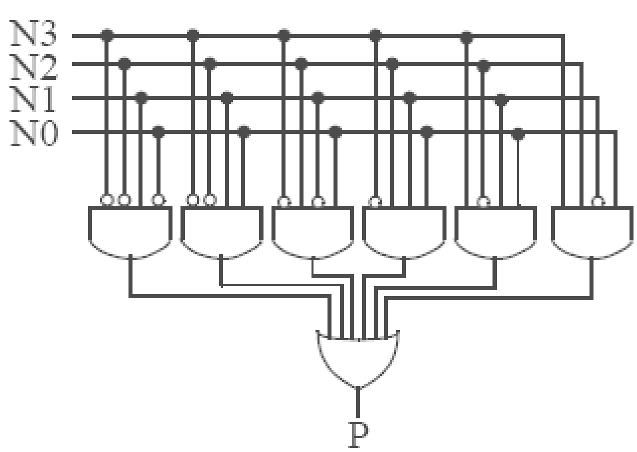
Inputs Outputs

N3	N2	N1	N0	P
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Step 2 - Convert to equations

P = N3’N2’N1N0’ + N3’N2’N1N0 + N3’N2N1’N0 + N3’N2N1N0 + N3N2’N1N0 + N3N2N1’N0

Step 3 - Implement as a gate-based circuit



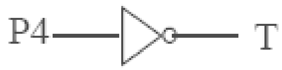
2.59 Step 1 - Capture the function

Skipped - we'll use an equation directly.

Step 2 - Convert to equations

T' = P4

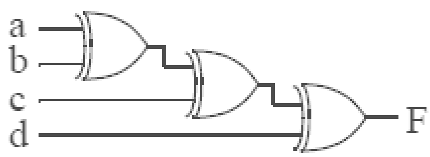
Step 3 - Implement as a gate-based circuit



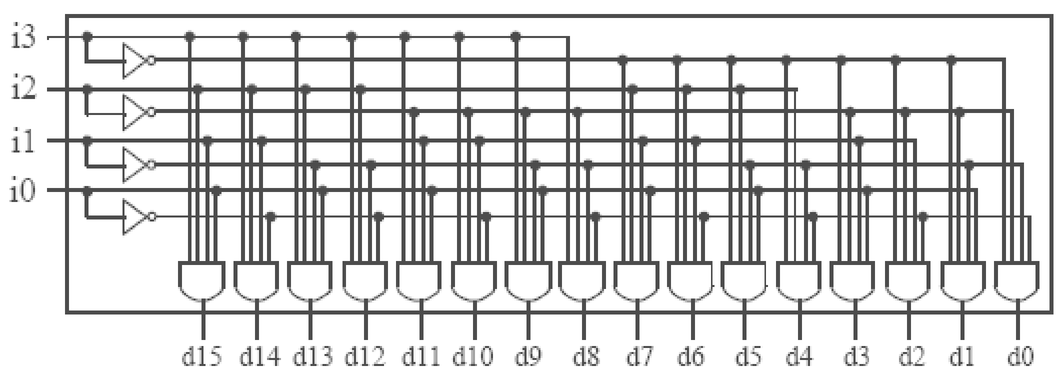
2.64

F = (a XOR b) + (c XOR d) + ac

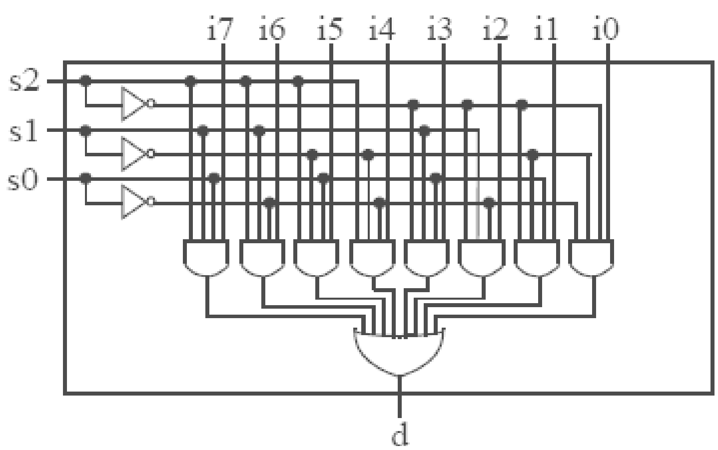
2.65



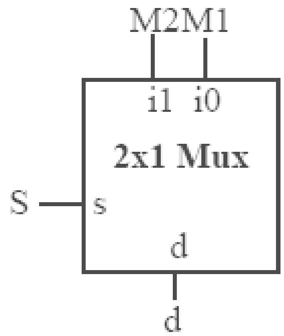
2.70



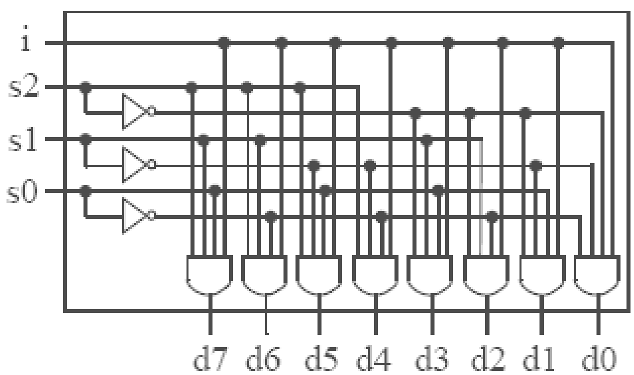
2.72



2.75



2.78

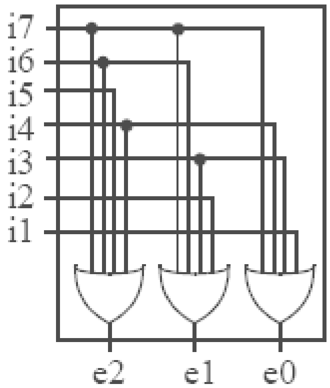


2.80

Inputs Outputs

i7	i6	i5	i4	i3	i2	i1	i0	e2	e1	e0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

e2 = I7 + I6 + I5 + I4
e1 = I7 + I6 + I3 + I2
e0 = I7 + I5 + I3 + I1



2.81

Inputs Outputs

i3	i2	i1	i0	e1	e0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

e1 = i3 + i2

e0 = i3 + i2’i1