

Student ID: \_\_\_\_\_

# CS 151 Quiz 4

Name : \_\_\_\_\_ , \_\_\_\_\_  
(Last Name) (First Name)

Student ID : \_\_\_\_\_

Signature : \_\_\_\_\_

## **Instructions:**

1. Please verify that your paper contains **10 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **60 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

Student ID: \_\_\_\_\_

**Q1: [ALU]**

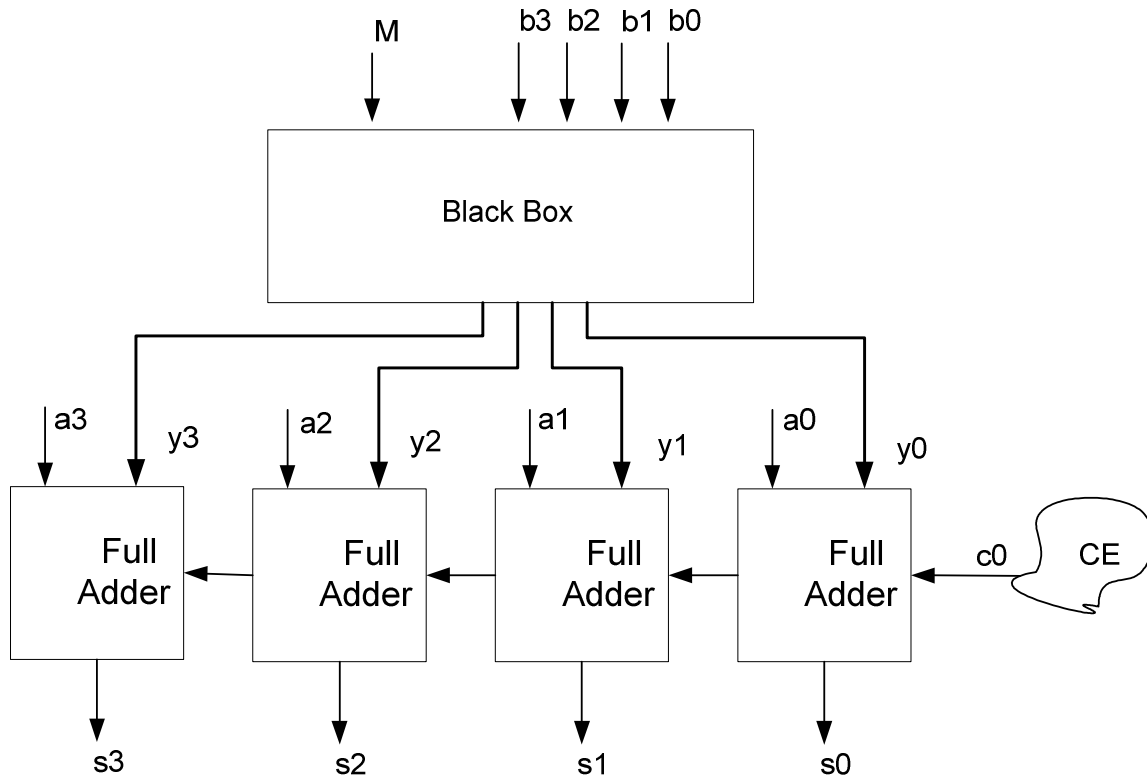
**[10 points]**

We are going to design a very simple 4-bit Arithmetic Unit (AU) with the following functional table:

M	Function Name	F(A,B)
0	Subtract B from A	A-B
1	Subtract 1 from A	A-1

A and B are two, 4-bit binary numbers  $a_3a_2a_1a_0$  and  $b_3b_2b_1b_0$ .  
M is the control input to this AU.

For doing this, the blocks labeled AE (Arithmetic Extender) and CE (Carry Extender) in the following block diagram should be designed:



a. Fill the following table for  $y_3, y_2, y_1, y_0$  and  $c_0$  based on the inputs of the AU which are  $a_3, a_2, a_1, a_0, b_3, b_2, b_1, b_0, M_1$  and  $M_0$ : [7 points]

M	$y_3$	$y_2$	$y_1$	$y_0$	$c_0$
0					
1					

Student ID: \_\_\_\_\_

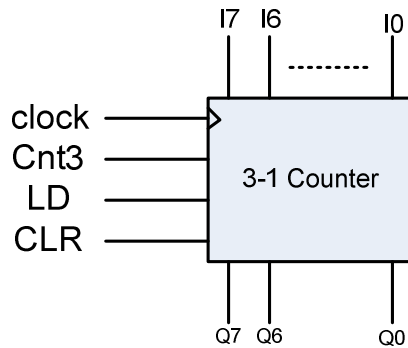
- b. Using the table that you derived in part (a), derive the logic equations for  $y_1$ ,  $y_0$  and  $c_0$ . [3 points]**

Student ID: \_\_\_\_\_

## Q2: RTL design

[35 points]

We want to design an 8-bit, 3-1 counter using RTL design method. The 8-bit, 3-1 counter has following block diagram and characteristics:



- a. “Cnt3” input: when Cnt3=1, it adds 3 to the current value, when Cnt3=0 it adds 1 to the current value
- b. “LD” input: when LD=1, it loads from input I[7:0] regardless of the value of Cnt3
- c. “CLR” input: when CLR=1, it clear the outputs (Q[7:0] = “00000000”) regardless of the value of LD or Cnt3

Student ID: \_\_\_\_\_

**1. Draw the Function Table. [5 points]**

**2. Capture a high-level state machine [10 points]**

Student ID: \_\_\_\_\_

- 3. Create the datapath (Hint: use a register, and an adder to do both increment)  
[10 points]**

Student ID: \_\_\_\_\_

**4. Connect the datapath to controller [5 points]**

Student ID: \_\_\_\_\_

**5. Derive the controller's FSM [5 points]**

Student ID: \_\_\_\_\_

**Q2: [Shift Register] [15 points]**

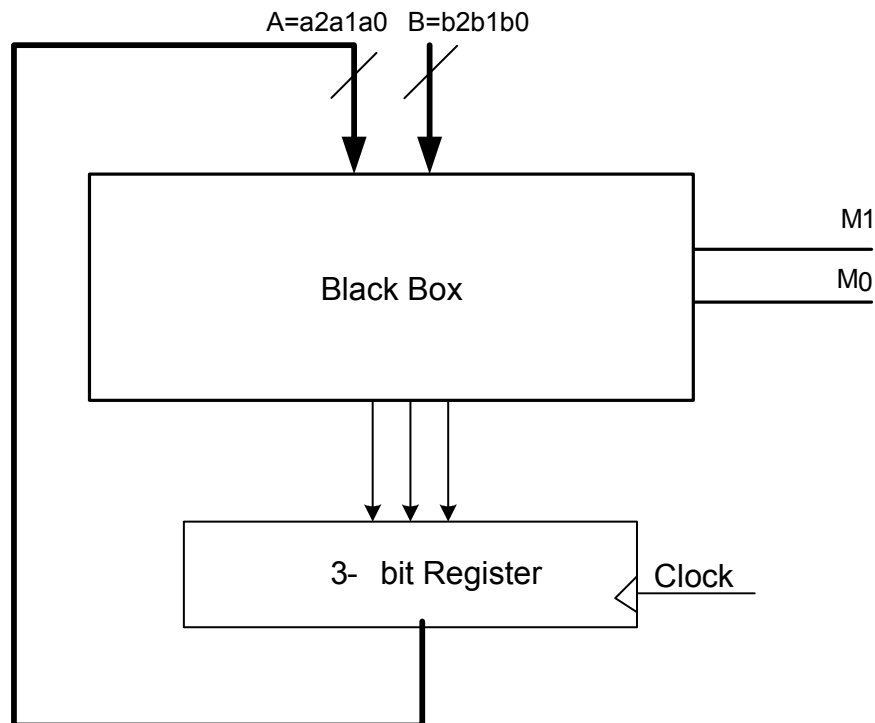
We want to design a 3-bit circular shift register by adding the circuit in the Black Box to a 3-bit register. By just using 4-to-1 Multiplexers design the Black Box in the figure.

M1M0 are control bits to this Circular Shift Register.

The value on load line is  $B = b_2b_1b_0$ .

**Function Table:**

M1	M0	Action	Register Current Value	Register Next Value
0	0	Keep current value	$A = a_2a_1a_0$	$a_2a_1a_0$
0	1	Rotate Shift Right by 1 bit	$a_2a_1a_0$	$a_0a_2a_1$
1	0	Load	$a_2a_1a_0$	$b_2b_1b_0$
1	1	Rotate Shift Right by 2 bits	$a_2a_1a_0$	$a_1a_0a_2$



Student ID: \_\_\_\_\_

<This page is intentionally left blank>