

Student ID: \_\_\_\_\_

# CS 151 Quiz 6

Name : \_\_\_\_\_ , \_\_\_\_\_  
(Last Name) (First Name)

Student ID : \_\_\_\_\_

Signature : \_\_\_\_\_

## **Instructions:**

1. Please verify that your paper contains **6 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **35 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

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**Question 1 [State minimization]**

**[15 points]**

- a. Reduce the number of states in the following state table using the implication table method. **(10 points)**

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
A	B	F	1	1
B	F	D	1	1
C	D	E	0	1
D	C	F	0	1
E	D	C	1	1
F	C	C	1	1

Notice that this state table is for a **Mealy** machine.

<u>A</u>						
<u>B</u>						
<u>C</u>						
<u>D</u>						
<u>E</u>						
<u>F</u>						
	<u>A</u>	<u>B</u>	<u>C</u>	<u>D</u>	<u>E</u>	<u>F</u>

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**b.** Tabulate the reduced state table using the table provided below. **(5 points)**

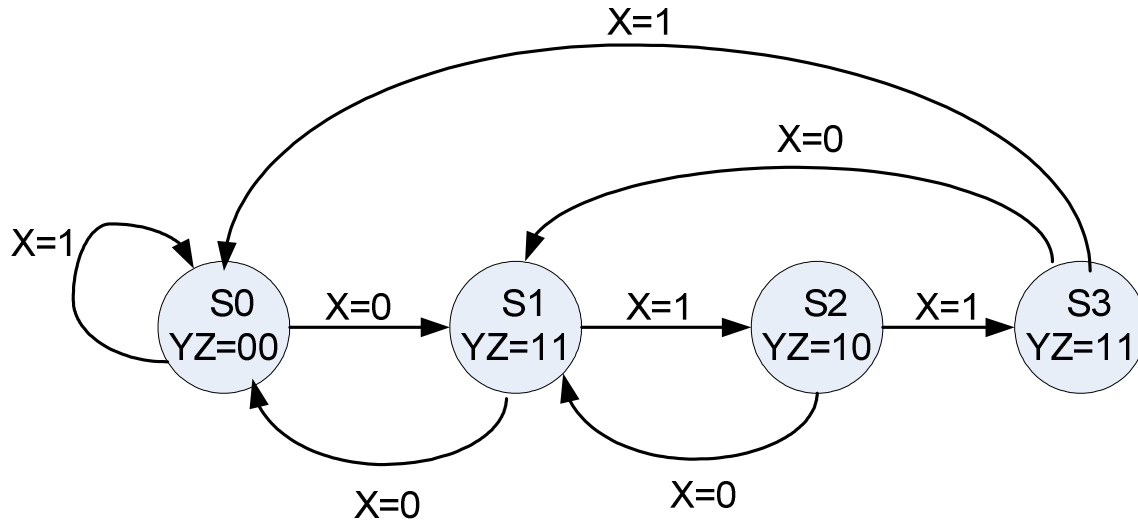
Present state	Next State		Output	
	X=0	X=1	X=0	X=1

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**Question 2 [State encoding]**

**[20 points]**

For the FSM given below:  
(Y and Z are the outputs of the FSM)



- a. Using the **binary** state encoding, draw the combinational circuit required to implement this FSM. **(5 points)**  
**(HINT: The combinational logic should be optimized before drawing the circuit.)**

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- b.** Calculate the area (*number of 2-input gates*) of the implementation and show the critical path and calculate the critical path delay (*number of 2-input gate levels*) **(3 points)**

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- c. Using the **one-hot** state encoding, draw the combinational circuit required to implement this FSM. **(5 points)**  
**(HINT: The combinational logic should be optimized before drawing the circuit.)**

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- d. Calculate the area (*number of 2-input gates*) of the implementation and show the critical path and calculate the critical path delay (*number of 2-input gate levels*) **(3 points)**

- e. Which design (a or b) is better for area? **(2 points)**

- f. Which design (a or b) is better for speed? **(2 points)**