

Student ID: _____

CS 151

Quiz 7

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **6 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **40 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

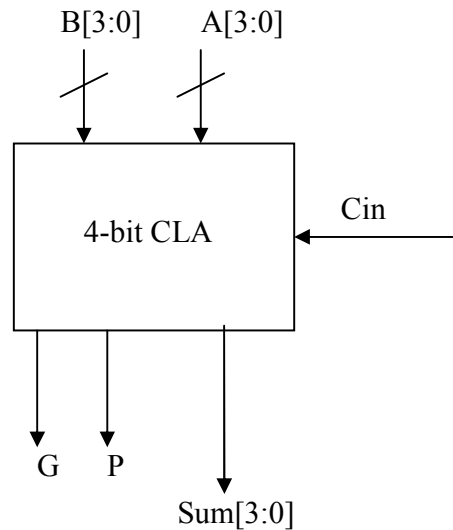
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[Carry Look-Ahead adder]

[40 points]

1. Design a 16-bit hierarchical carry look-ahead following steps (1.a) and (1.b), using 4-bit carry look-ahead adders shown below.

In this Question use one level of hierarchy. (15 points)



- a) Draw the interface between the 4-bit CLAs and the CLA Logic that should be added to implement the 16-bit adder. (At this stage you do not need to implement the circuit inside the blocks.) **(5 points)**

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b) Write the equations for the outputs of the CLA Logic block. (10 points)

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2. Design a 16-bit hierarchical carry look-ahead following steps (2.a) and (2.b), using 4-bit carry look-ahead adders shown in page 2.

In this Question use two levels of hierarchy. (15 points)

(HINT: In this example you should first design 8-input adders and then combine the adders to design a 16-bit adder)

- a) Draw the block structure of the 16-bit adder and show the interface signals between the blocks. (At this stage you do not need to implement inside the blocks.) **(5 points)**

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- b) Write the equations for the outputs of the CLA Logic blocks in each level.
(10 points)

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3. Assuming that the delay of a 4-bit adder is α , and the delay of a 2-input gate is β , and the area of a 2-input gate is X and the area of a 4-bit adder is Y , compare the two designs in Question 1 and Question 2 with respect to their area and critical path delay. **(10 points)**

(HINT: only 2-input gates can be used to implement the additional carry-look ahead circuit.)

a) Delay of design 1 =

Area of design 1 =

b) Delay of design 2 =

Area of design 2 =