

Student ID: \_\_\_\_\_

# CS 151 Quiz 2

Name : \_\_\_\_\_ , \_\_\_\_\_  
(Last Name) (First Name)

Student ID : \_\_\_\_\_

Signature : \_\_\_\_\_

## **Instructions:**

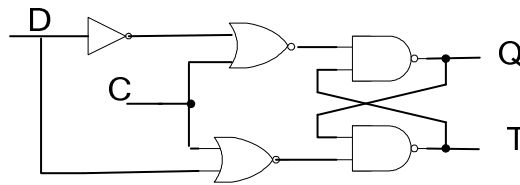
1. Please verify that your paper contains **4 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **30 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

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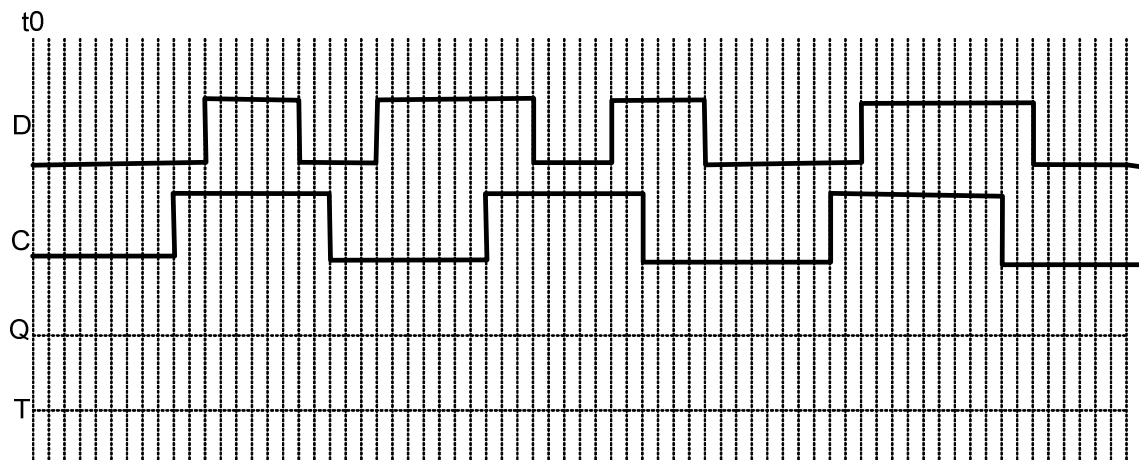
**Q1: [Latch analysis]**

**[10 points]**

Shown below is a NAND implementation of gated D-latch:



The timing diagrams of D and C are shown below. Show the timing diagram for Q and T:  
(Assume that  $Q=1$  and  $T=0$  at  $t_0$  and there is no gate delay)

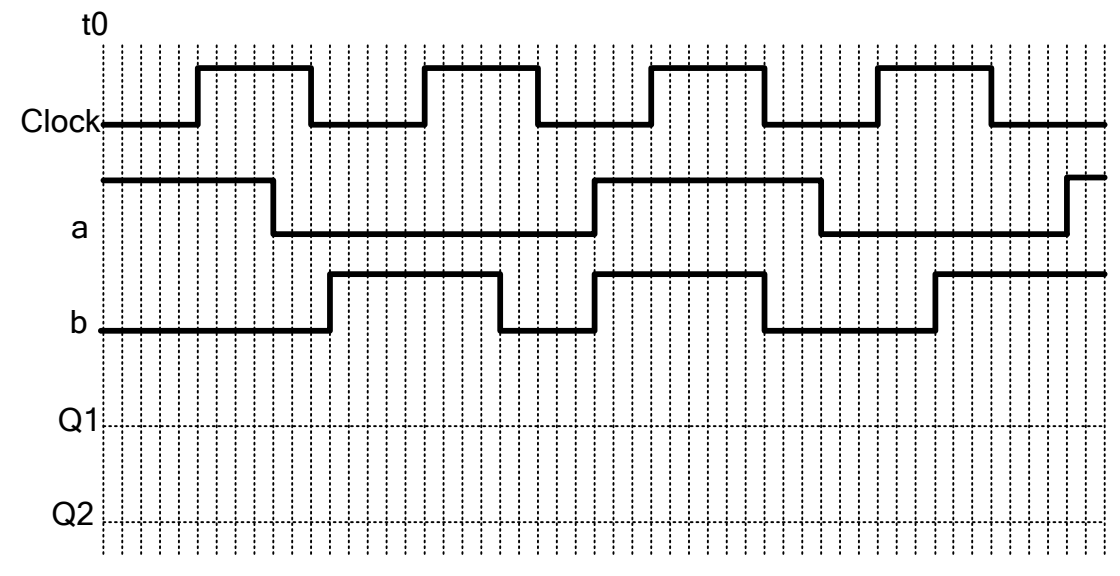
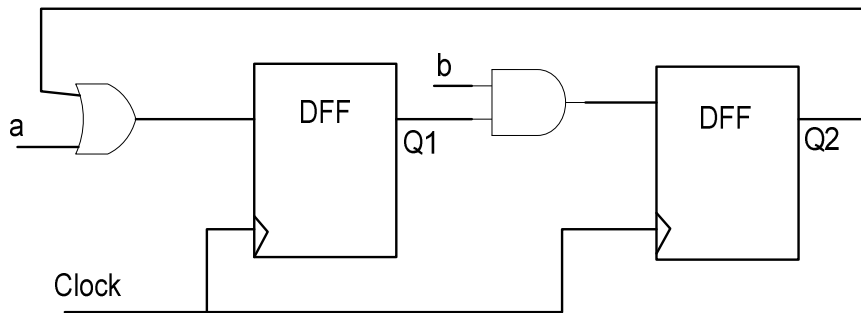


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**Q2: [Sequential Circuit Timing Analysis]**

**[10 points]**

The circuit below shows a sequential circuit using D Flip Flops. Assuming that “a” and “b” are the inputs of the circuit, and Q1 and Q2 are initially 0, show the timing diagram for Q1 and Q2. NOTE: You can assume that gate delay is negligible.



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**Q3: [FSM design]**

**[10 points]**

An elevator has a counter to identify the limit on the number of people who can get in. A pulse generator generates a pulse if someone gets in the elevator. If the number of people reaches the limit of 4 then a red light illuminates and no one else can get in. Design the FSM for the controller of this elevator.