

Student ID: _____

CS 151 Quiz 6

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **9 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **45 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

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Question 1 [State minimization]

[15 points]

- a. Reduce the number of states in the following state table using the implication table method. (10 points)

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	D	C	0	1
C	E	D	0	1
D	E	C	0	1
E	D	C	1	1

Notice that this state table is for a **Mealy** machine.

<u>A</u>					
<u>B</u>	X				
<u>C</u>	X	(E, D) (D, C)			
<u>D</u>	X	(E, D) (C, C)	(E, E) (C, D)		
<u>E</u>	X	X	X	X	
	<u>A</u>	<u>B</u>	<u>C</u>	<u>D</u>	<u>E</u>

States C and D are equal.

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b. Tabulate the reduced state table using the table provided below. (5 points)

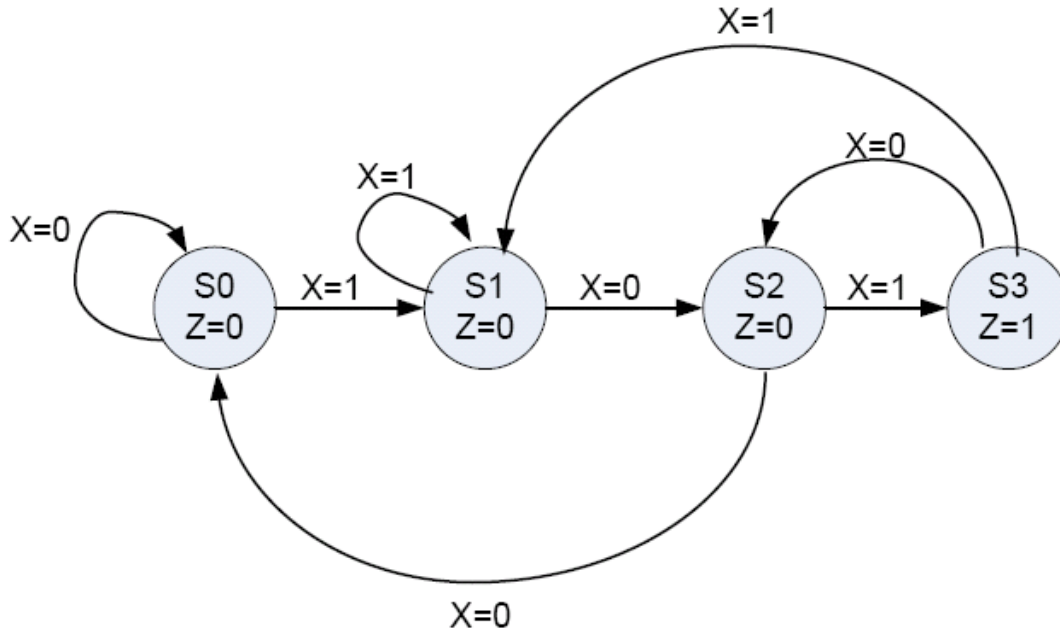
Present state	Next State		Output	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	CD	CD	0	1
CD	E	CD	0	1
E	CD	CD	1	1

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Question 2 [State encoding]

[20 points]

For the FSM given below:
(Z is the output of the FSM)



- a. Using the **binary** state encoding, draw the combinational circuit required to implement this FSM. (5 points)
(HINT: The combinational logic should be optimized before drawing the circuit.)

S0 = 00, S1 = 01, S2 = 10, S3 = 11

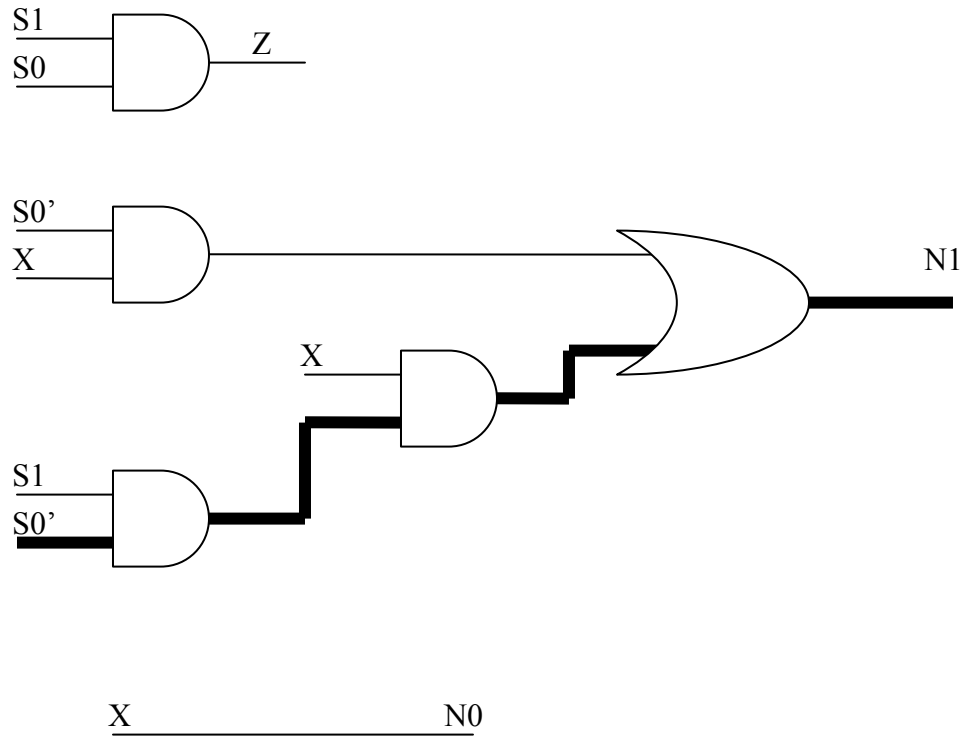
Current State		Input X	Next State		Output Z
S1	S0		N1	N0	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	0	1	1

$$Z = S1S0$$

$$N1 = S1'S0X' + S1S0'X + S1S0X' = S1S0'X + S0X'$$

$$N0 = S1'S0'X + S1'S0X + S1S0'X + S1S0X = X$$

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- b. Calculate the area (*number of 2-input gates*) of the implementation and show the critical path and calculate the critical path delay (*number of 2-input gate levels*) (3 points)

The area consists of 5, 2-input gates. The critical path is shown in the previous figure and the critical path delay is 3 gate delays.

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- c. Using the **one-hot** state encoding, draw the combinational circuit required to implement this FSM. (5 points)
(HINT: The combinational logic should be optimized before drawing the circuit.)

$S_0 = 0001, S_1 = 0010, S_2 = 0100, S_3 = 1000$

Current State				Input	Next State				Output
S3	S2	S1	S0	X	N3	N2	N1	N0	Z
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	0	1	0	0	0
0	0	1	0	1	0	0	1	0	0
0	1	0	0	0	0	0	0	1	0
0	1	0	0	1	1	0	0	0	0
1	0	0	0	0	0	1	0	0	1
1	0	0	0	1	0	0	1	0	1

$$N_3 = S_2X$$

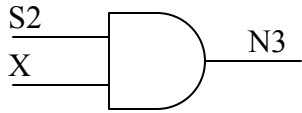
$$N_2 = S_1X' + S_3X'$$

$$N_1 = S_0X + S_1X + S_3X$$

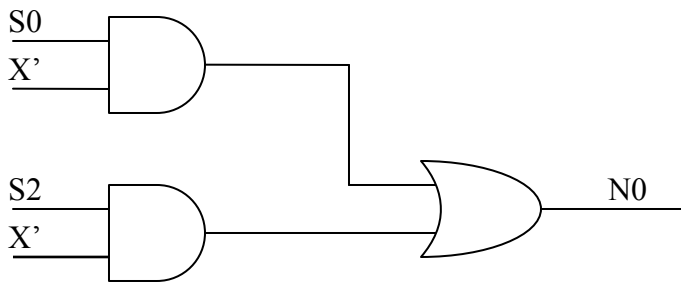
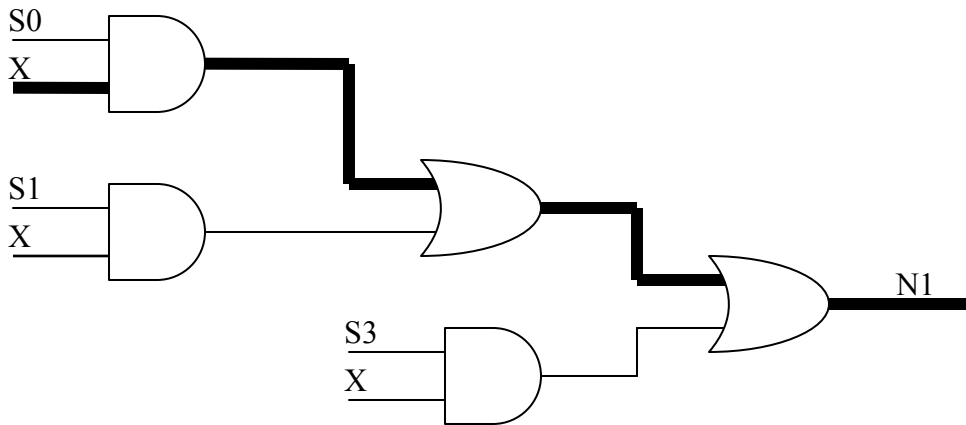
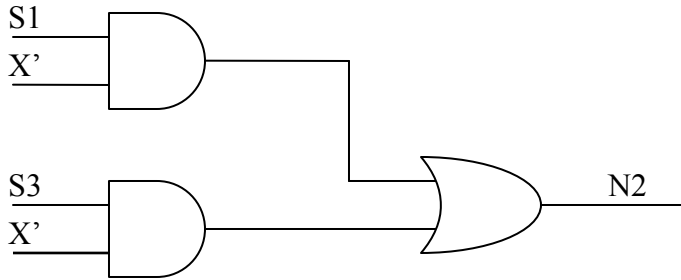
$$N_0 = S_0X' + S_2X'$$

$$Z = S_3$$

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$S3$ _____ Z



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- d.** Calculate the area (*number of 2-input gates*) of the implementation and show the critical path and calculate the critical path delay (*number of 2-input gate levels*) **(3 points)**

12, 2-input gates have been used. The critical path is shown in the previous figure and the critical path delay is 3 gated-delays.

- e.** Which design (a or b) is better for area? **(2 points)**

Design a is better for area.

- f.** Which design (a or b) is better for speed? **(2 points)**

Both designs have the same amount of delay.

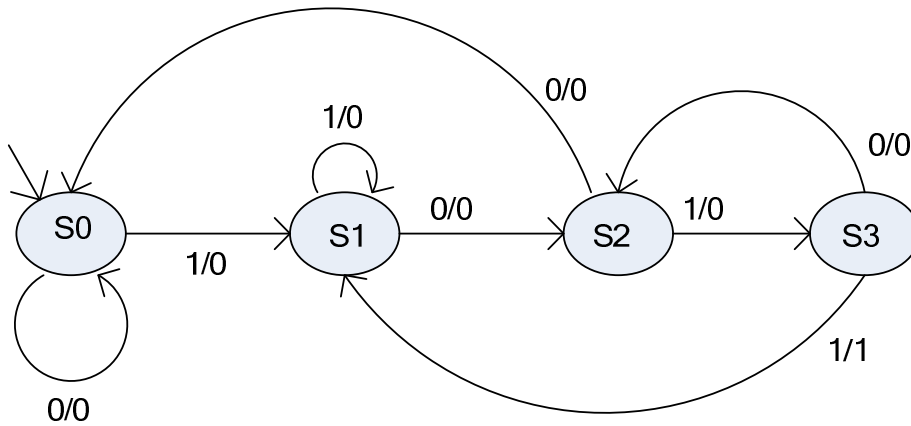
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Question 3 [Mealy Machine Design]

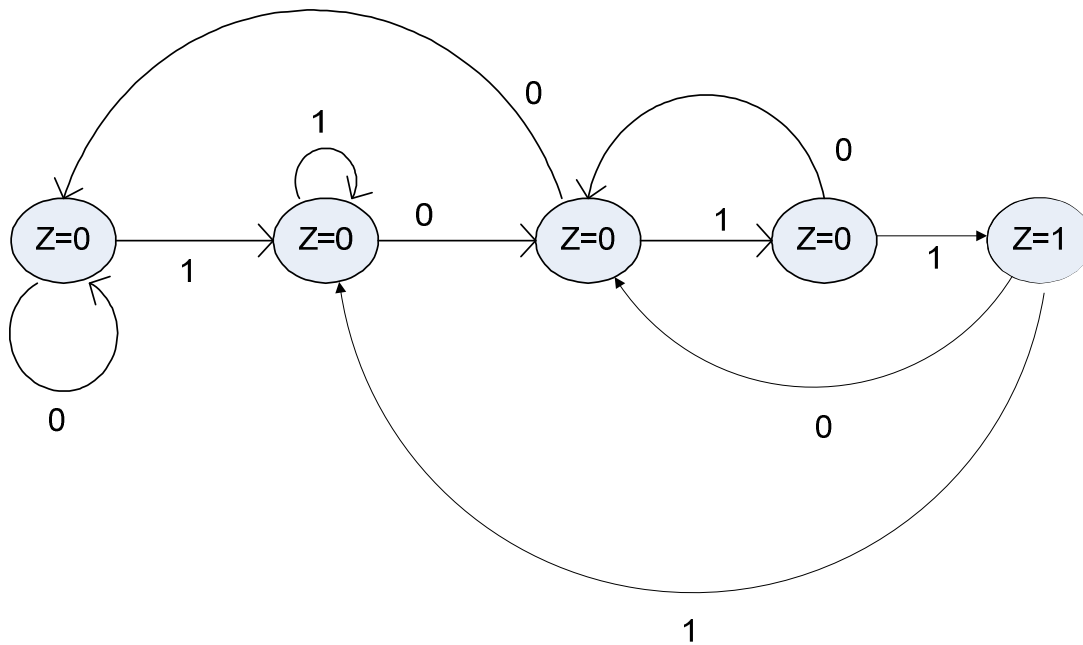
[10 points]

In the following Mealy state machine, assuming that X is the input and Y is the output of the FSM, convert the state machine to a Moore machine.

Note: Transitions are of the form X/Y.



Answer:



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