

Student ID: _____

CS 151 Quiz 2

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **5 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **35 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

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Q1: [Mux/Decoder application]

[15 points]

For function $F(x,y,z) = x'yz + xy'z' + x'yz' + xy'z$:

(a) Implement **F** by means of a 4-to-1 multiplexer (8 points)

(HINT: You can use NOT gates to invert the input to the MUX)

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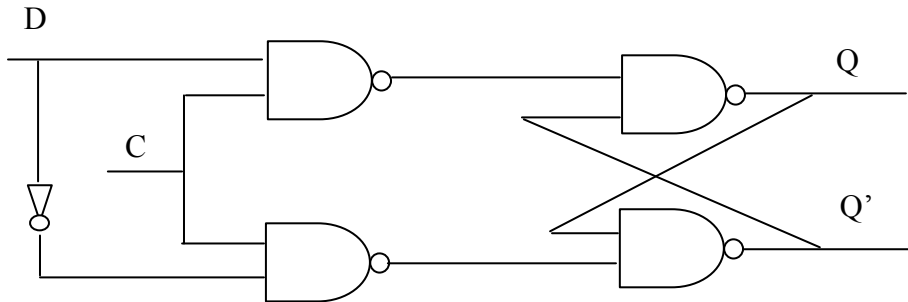
(b) A 3-to-8 decoder (7 points)

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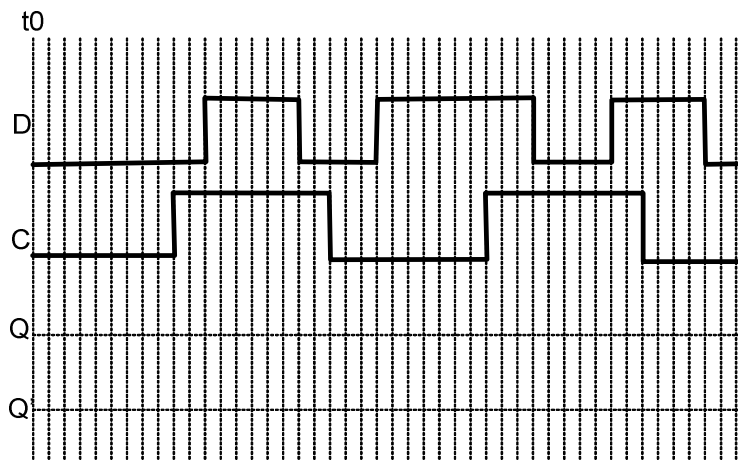
Q2: [Latch analysis]

[10 points]

Shown below is a NAND implementation of gated D-latch:



The timing diagrams of D and C are shown below. Show the timing diagram for Q and Q': (Assume that Q=0 at t₀ and there is no gate delay)

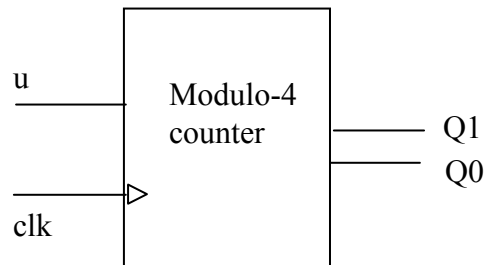


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Q3: [FSM design]

[10 points]

We want to design a binary up/down modulo-4 counter. A counter has an input “u”. A modulo-4 counter counts from 0 to 3 and then it starts from “0” ($0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 0 \rightarrow 1 \dots$). When $u=1$, the counter counts up from current value and when $u=0$, the counter counts down from current value ($3 \rightarrow 2 \rightarrow 1 \rightarrow 0 \rightarrow 3 \rightarrow 2 \dots$) and so on.



Show the value of output for the following given values for “u”

u: 1 → 1 → 1 → 1 → 0 → 0 → 1 → 1 → 0

Q_1Q_0 : 00 → 01 →

Design the FSM for this counter.