

Student ID: _____

CS 151 Quiz 3

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

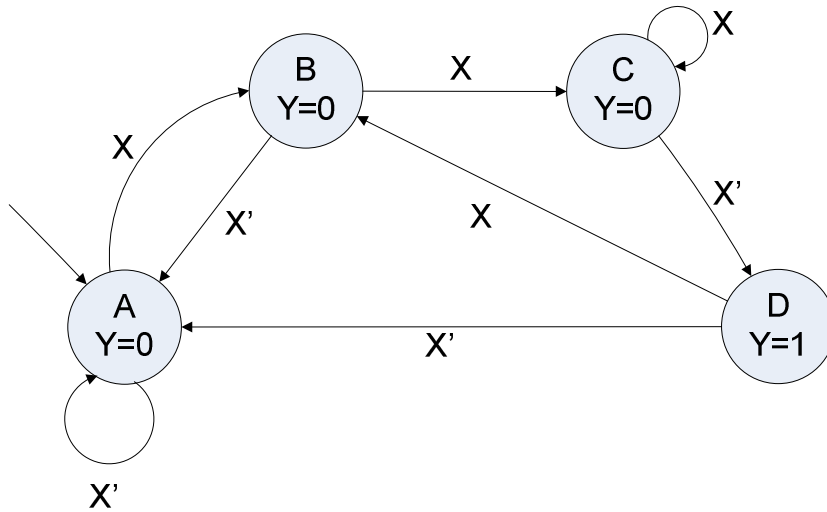
1. Please verify that your paper contains **5 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **40 points**.
5. To receive credit you must show your work clearly.
6. **For possible re-grade request make sure that your write clearly.**
7. Calculators are **NOT** allowed.

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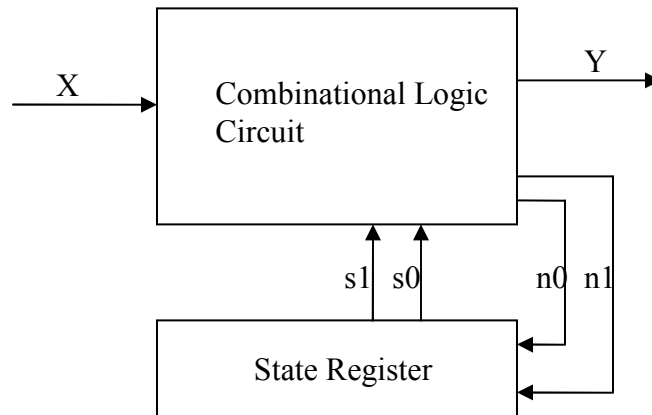
Q1: [Controller Design]

[15 points]

Considering the FSM shown below:
(X is the input and Y is the output of the FSM.)



a) Create the architecture for this FSM. [5 points]



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b) Considering the state encoding shown below, draw the state table. [10 points]

A = 00, B = 01, C = 10, D = 11

NOTE: You don't need to write the equations.

Current State		Input	Next State		Output
S1	S0	X	N1	N0	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	1	1

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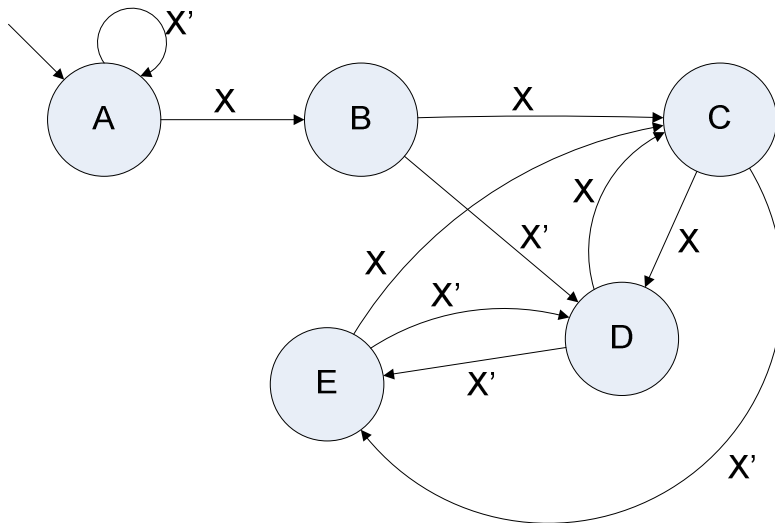
Q2: [Reverse Engineering]

[10 points]

Considering the state table below and the corresponding encoding of the states, design the FSM.

Present state	Next State		Output
	X=0	X=1	
000	000	001	0
001	011	010	1
010	100	011	1
011	100	010	1
100	011	010	0

- A = 000
- B = 001
- C = 010
- D = 011
- E = 100



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Q3: [Registers]

[15 points]

Design inside the Black Box below to implement a 4-bit register with the functionality specified in the following table. ($A = a_3a_2a_1a_0$ is the output of the register.)

NOTE: Specify the select lines of each multiplexer as well as the inputs. You can use one of the following components if needed.

- Adder
- Comparator
- Counter

S_1S_0	Action	Output
00	Load	$b_3b_2b_1b_0$
01	Keep current value	A
10	Multiply by 2	$A*2$
11	Add 1 to A	$A+4$

