

Student ID: _____

ICS 151 Midterm

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

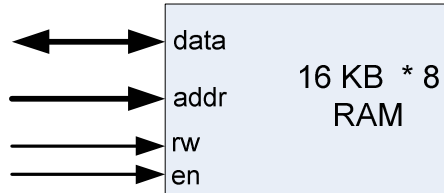
1. Please verify that your paper contains **5 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this midterm are **30 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

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Q1: Memory hierarchy

[10 points]

Design a 64 KB*32-bit RAM using only 16 KB*8-bit RAM modules and minimum number of logic components.



16KB*8-bit RAM Module

Logic Components

- a. Priority encoder
- b. Decoder
- c. Multiplexer

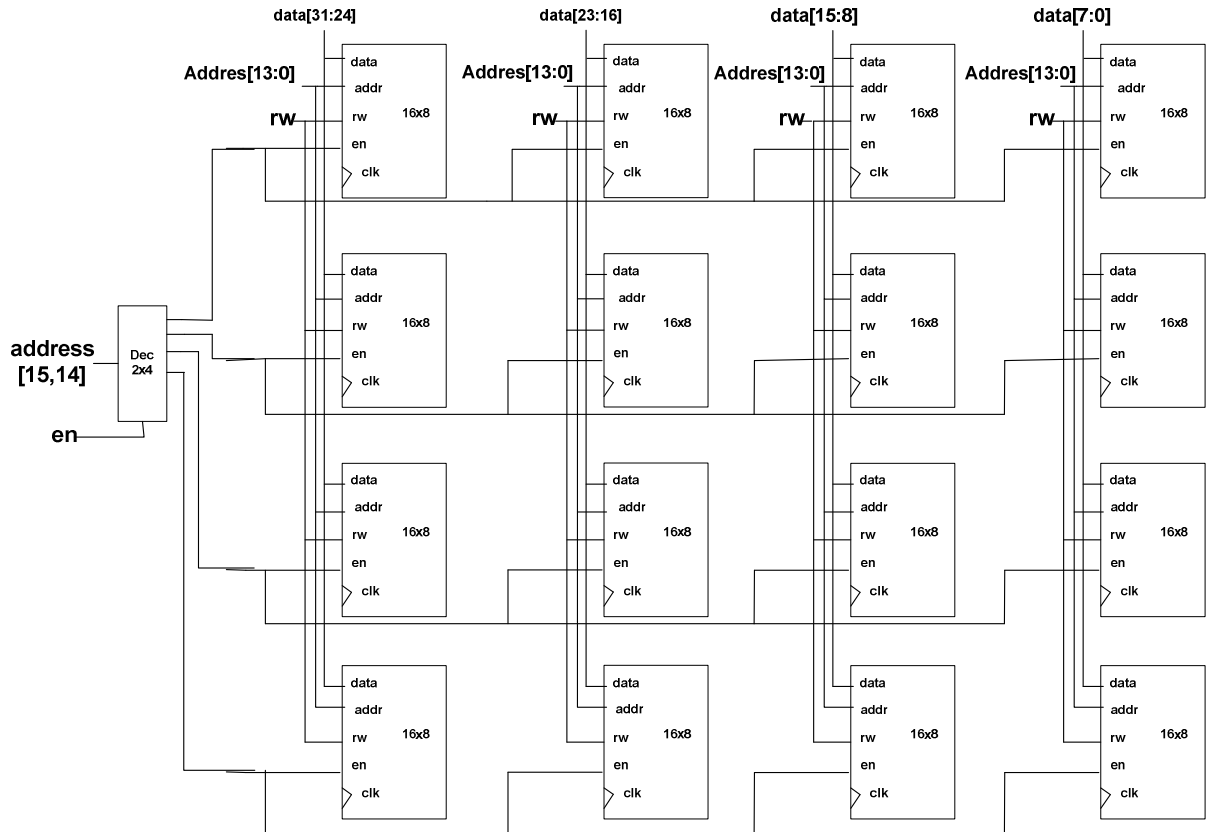
a. How many of each component is used?

of decoder : 1

of RAM module : 16

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b. Draw the whole circuit.



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Q2: Circuit Design

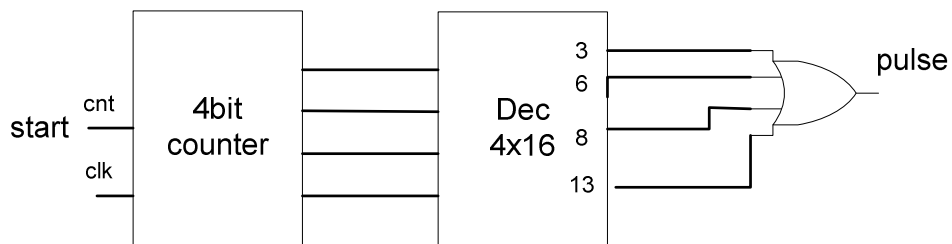
[20 points]

Design a circuit that is activated on a “START” signal and outputs a signal “PULSE” on a regular interval as described below.

The circuit cycles through 16 clock cycle periods (0 through 15 cycles) and asserts PULSE on clock cycles 3, 6, 8, 13.

- a. (Component Use) Design this circuit using the following components
- Counter
 - Decoder
 - Logic gates

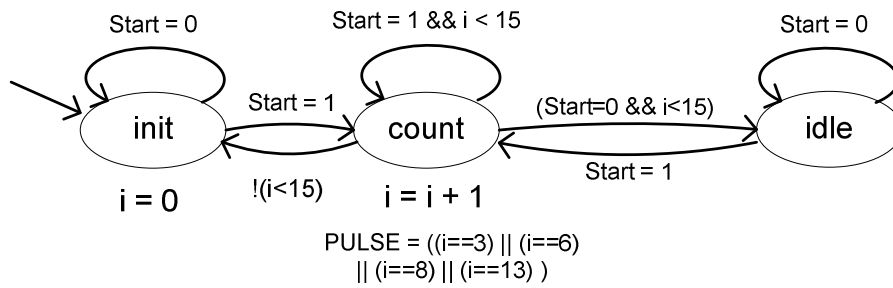
(HINT: use the counter component with additional logic; DON'T use the RTL design methods for this part):



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- b. (RTL-based Design) Now design this circuit using the RTL design method. Only do Step 1, i.e., capture the high-level state machine (FSMD).

1) If 'START' acts like an enabling signal (like the solution in part a)



2) If 'START' only initiates the process for a period of 16 clock cycles:

