

Student ID: _____

ICS 151 Quiz 3

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **10 pages** including this cover and blank pages.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book. No notes or other materials** are permitted.
4. Total credits of this midterm are **40 points**.
5. To receive the whole credit, you must show your work clearly.
6. Calculators are **NOT** allowed.

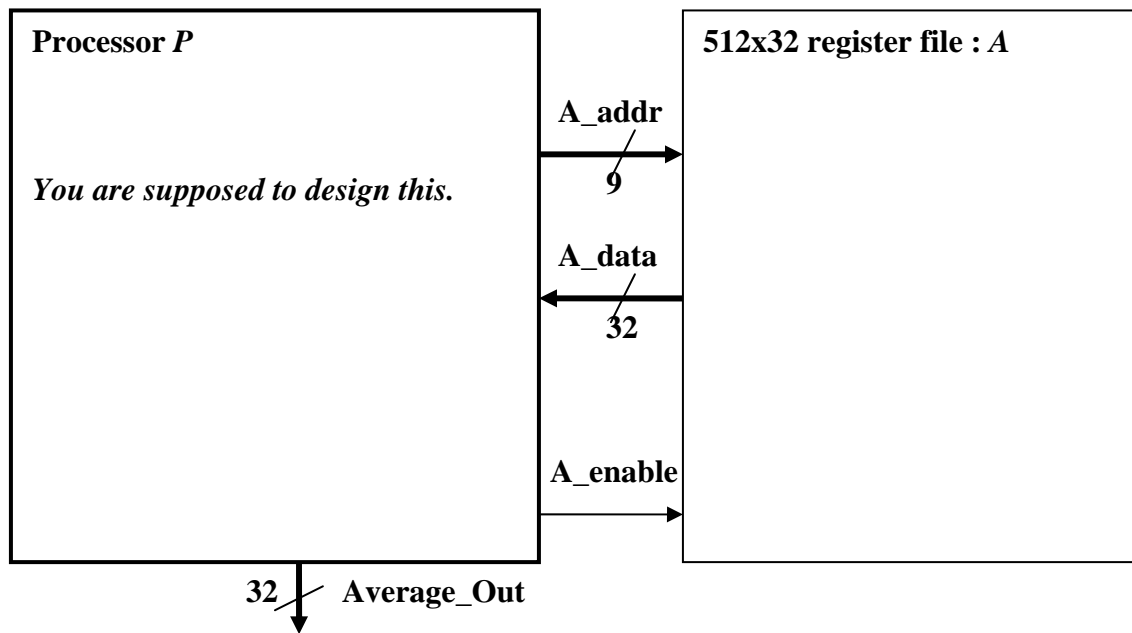
Q1: RTL Design

[30 points]

Using RTL design method, we want to design a processor “P”, consisting of a data path and a controller that computes the average of all 512 32-bit numbers stored in a 512x32 register file “A”.

Between the processor “P” and the register file “A”, there are three connections like A_enable, A_addr, and A_data as shown in the graph below. When A_enable = 1, the processor “P” can read one 32-bit data through A_data from one register with 9-bit A_addr in “A”. When A_enable = 0, we can not read the data from “A”.

[For simplicity, register file A has only A_data, A_addr and A_enable for READ. We do not consider WRITE operation for “A”]



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(a) Capture a high-level state machine [10 points]

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(b) Create the datapath [10 points]

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(c) Connect the datapath to the controller [5 points]

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(d) Derive the controller's FSM [5 points]

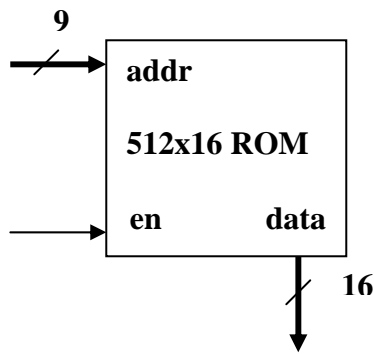
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Q2: Memory Hierarchy **[10 points]**

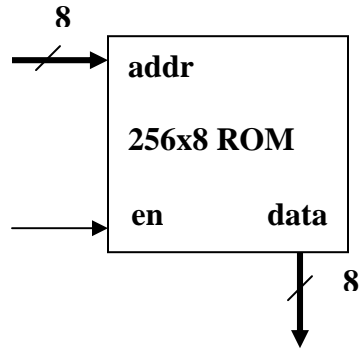
We want to design ROM in a hierarchical way, composing larger components from smaller components.

- (a) Compose 1024x16 Rom using only 512x16 ROMs. [5 points]
(NOTE: YOU NEED TO SPECIFY THE NUMBER OF BITS FOR ALL DATA AND CONTROL SIGNALS)



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(b) Compose 256x16 ROM using only 256x8 ROMs. [5 points]
(NOTE: YOU NEED TO SPECIFY THE NUMBER OF BITS FOR ALL DATA AND CONTROL SIGNALS)



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