Student ID: _____

ICS 151
Final

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **9 pages** including this cover and 3 blank pages.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **40 points.**
5. To receive the whole credit you must show your work clearly.
6. Calculators are **NOT** allowed.

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Q 1: Logic Optimization [20 points]

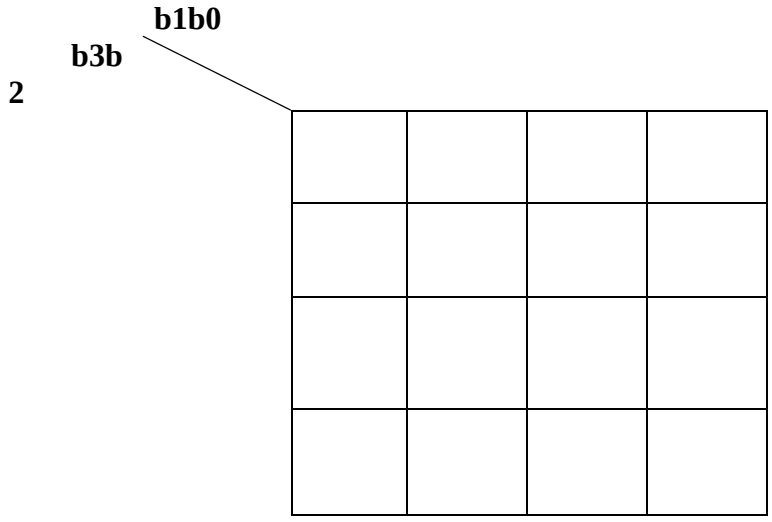
Design a circuit that accepts a 4-bit BCD (Binary Coded Decimal) digit and outputs 1 if the number is an odd number less than 6 or greater than 8.

[Notice that BCD is one representation form in which each integer of a decimal number is represented by a 4-bit binary number. For example, binary number (**b3b2b1b0 = 0011**) represents 3 in decimal (**d = 3**)]

a. Draw the truth table for this function. **[5 points]**

Binary				**Decimal**	**Output**
b3	**b2**	**b1**	**b0**	**d**	**F**
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	9	
1	0	1	0	don’t care	
1	0	1	1	don’t care	
1	1	0	0	don’t care	
1	1	0	1	don’t care	
1	1	1	0	don’t care	
1	1	1	1	don’t care	

b. Draw the K-map for this function. **[5 points]**



c. Show all the "**Prime Implicants**" and "**Essential Prime Implicants**".
[5 points]

d. Simplify the function **[5 points]**

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Q 2: State Minimization [10 points]

Reduce the number of states in the following state table using **the implication table method** and tabulate the reduced state table.

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	D	C	0	1
C	E	D	0	1
D	E	C	0	1
E	D	C	1	1

[Notice that this state table is for a **Mealy** machine.]

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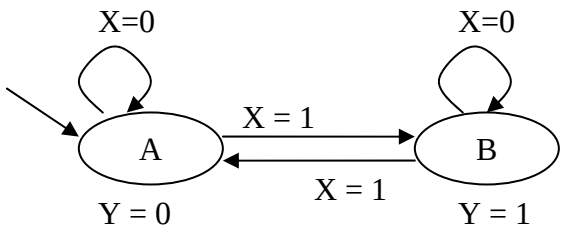
Q 3: State Encoding [10 points]

For the FSM given below:



a. Using the **binary** state encoding, implement the circuit and calculate the area (*number of 2-input gates*) and critical path delay (*number of 2-input gate levels*) **[5 points]**

b. Using a **one-hot** state encoding, implement the circuit and calculate the area (number of 2-input gates) and critical path delay (number of 2-input gate levels). **[5 points]**

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