

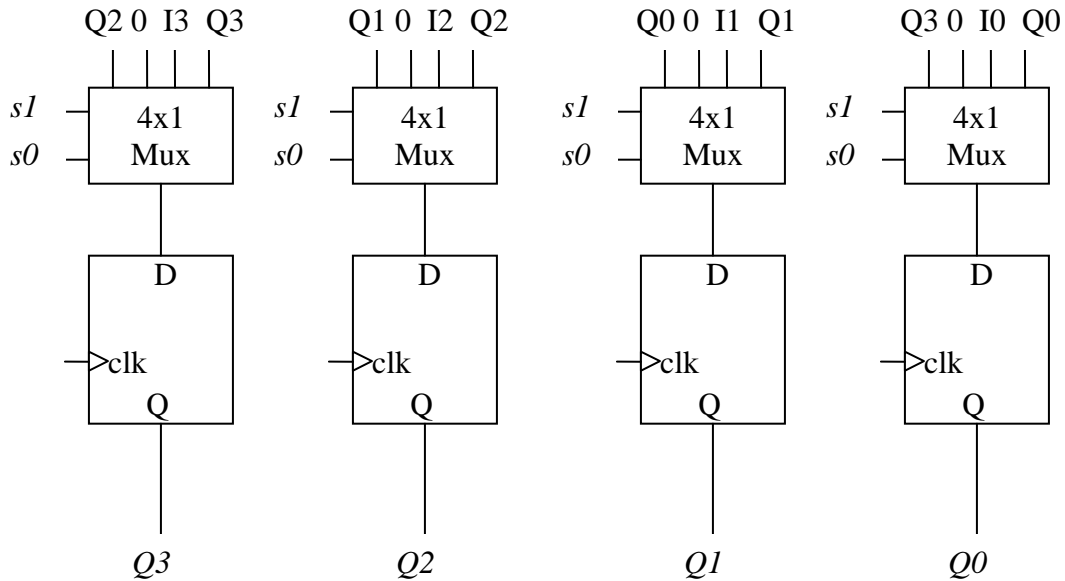
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Q1: Register Design

[10 points]

Design a 4-bit register with 2 control inputs s_1 and s_0 , 4 data inputs $I_3..I_0$, and 4 data outputs $Q_3..Q_0$. If $s_1s_0 = 00$, it means maintain the present value, $s_1s_0 = 01$ means load, and $s_1s_0 = 10$ means clear. $s_1s_0 = 11$ means to rotate left by 1, so 0101 would become 1010 and 1000 would become 0001.

[HINT: use D-Flip Flops and Mux]



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Q2: FSM Design

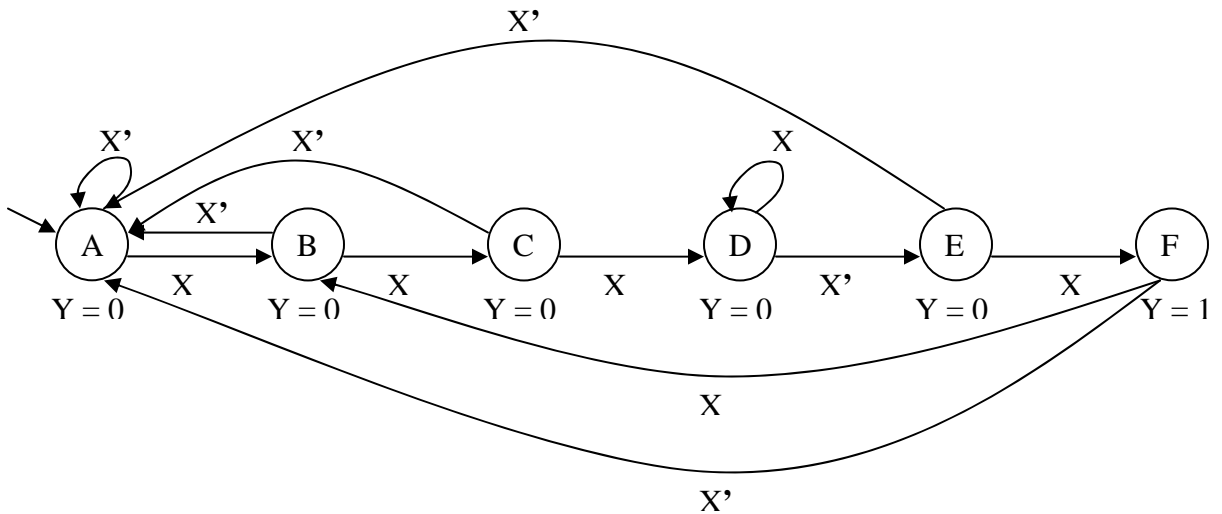
[20 points]

Design a state diagram for a recognizer that recognizes an input sequence **11101**. It has an input X and output Y. The recognizer sets the output to 1 (**Y = 1**) for exactly one clock cycle if the last five values on the input X were **11101**.

a. For the given input sequence, define the output sequence; (2 points)

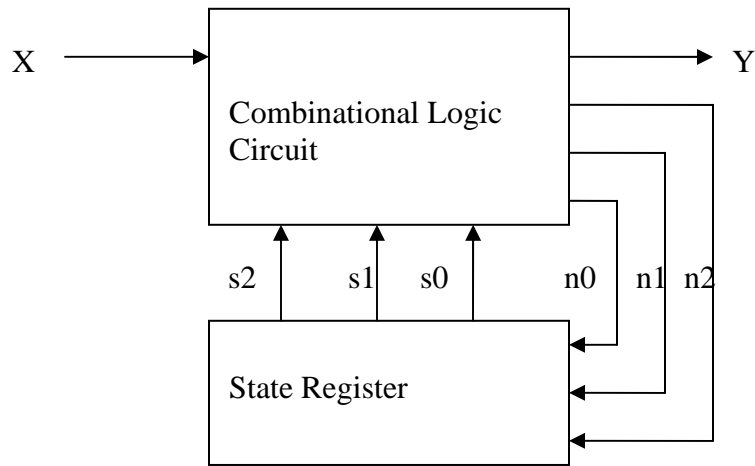
X	1	0	0	1	1	1	0	0	1	1	1	0	1	1	1	0	1	0	1	1	1
Y	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

b. Capture the FSM. (8 points)



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c. Create the architecture (3 points)



d. Encode the states (2 points).

- A = 000
- B = 001
- C = 010
- D = 011
- E = 100
- F = 101

e. Create the state table (5 points).

Present State			Input	Next State			Output
s2	s1	s0	X	n2	n1	n0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	1	1	0
0	1	1	0	1	0	0	0
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	1

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Q3: Circuit Design

[10 points]

Design a circuit that is activated on a “**START**” signal and outputs a signal “**PULSE**” on a regular interval as described below.

The circuit cycles through 16 clock cycle periods (0 through 15 cycles) and asserts “**PULSE**” on clock cycles 1, 7, 8, 15. Design this circuit using the following components:

- 4-bit Counter
- Decoder
- Logic gates

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Q4: Combinational Component Design **[10 points]**

Design a combinational component that implements the following function:

$$F(x,y) = \begin{cases} 3x > 4y \\ 2x+5y \\ \text{else} \\ 2x-y \end{cases}$$

Use the following components:

- Adder
- Subtractor
- Shifter
- Comparator
- Multiplexer

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Q5: ALU Design

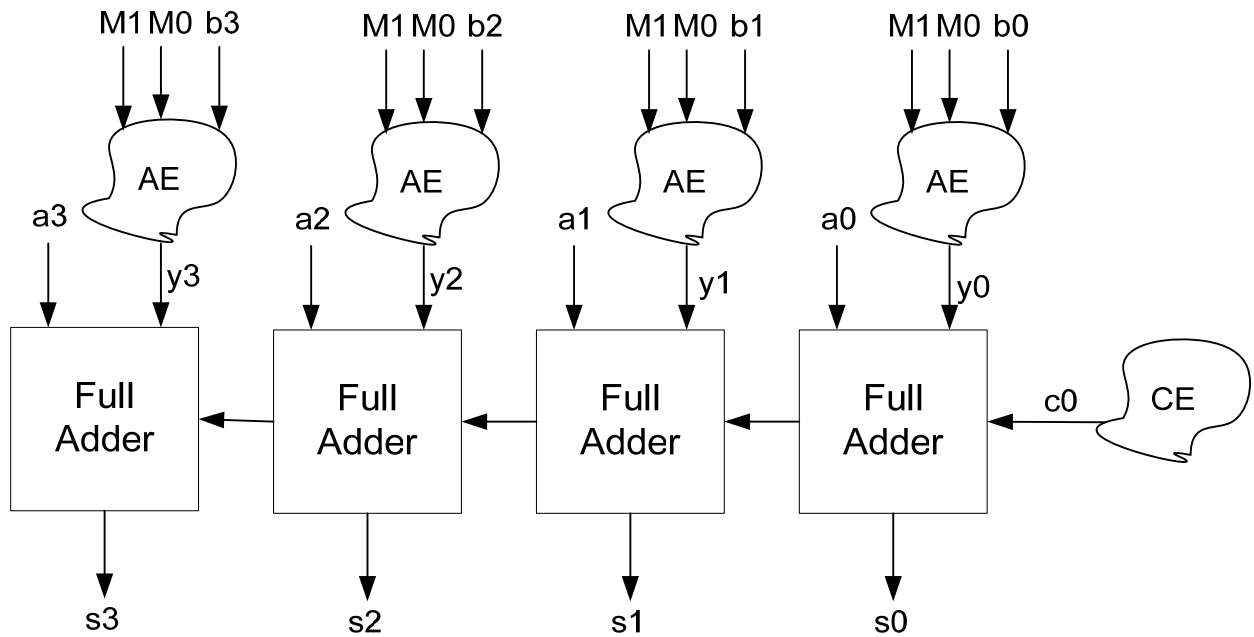
[20 points]

We are going to design a 4-bit Arithmetic Unit (AU) with the following functional table:

M1	M0	Function Name	F(A,B)
0	0	Add A and B	A+B
0	1	Subtract 2 times B from A	A-2*B
1	0	Increment A	A+1
1	1	Add 4 times B and A	A + 4*B

A and B are two 4-bit binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$.
M1, M0 are the control inputs to this AU.

For doing this, the blocks labeled AE (Arithmetic Extender) and CE (Carry Extender) in the following block diagram should be designed:



- a. Fill the following table for y_3, y_2, y_1, y_0 and c_0 based on the inputs of the AU which are $a_3, a_2, a_1, a_0, b_3, b_2, b_1, b_0, M_1$ and M_0 : (10 points)

M1	M0	y_3	y_2	y_1	y_0	c_0
0	0					
0	1					
1	0					
1	1					

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- b. Using the table that you reached in part (a), derive the logic equations for **y1**, **y0** and **c0**. (10 points)

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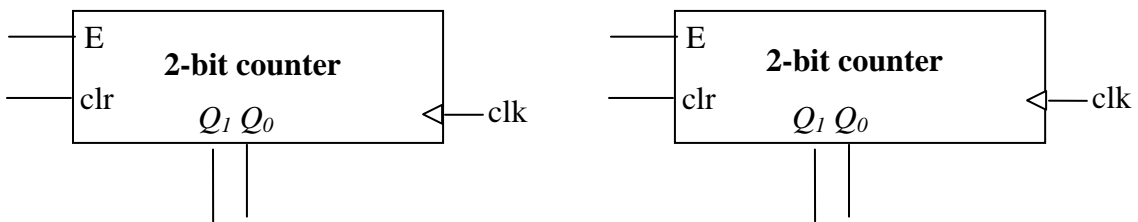
Q6: Counter Design

[10 points]

Design a 4-bit counter using two 2-bit counters. You may use logic gates as well.

E is enable input. When **E=1**, it counts at every clock cycle. When **E=0**, it stops counting and output stays unchanged.

clr is clear input. When **clr=1**, it starts counting from 0 from the next clock cycle if **E=1**.



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