

Student ID: \_\_\_\_\_

# ICS 151

## Quiz 5

Name : \_\_\_\_\_ , \_\_\_\_\_  
(Last Name) (First Name)

Student ID : \_\_\_\_\_

Signature : \_\_\_\_\_

### **Instructions:**

1. Please verify that your paper contains **5 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **40 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

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**Q1: RTL design** **[40 points]**

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**Design a circuit that sort 64 32-bit unsigned numbers stored in a 32x64 register file in increasing order. The design begins operation when a signal START is set to "1" and asserts signal DONE when the operation is completed.**

- 1. Capture a high-level state machine** **[10 points]**

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**2. Create the datapath using the components (as many as needed) listed below:**

- a. Register file (2 read port, 2 write port)**
- b. Adder**
- c. Comparator**
- d. Register**

**[10 points]**

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**3. Connect the datapath to controller**

**[5 points]**

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**4. Derive the controller's FSM diagram**

**[5 points]**