Student ID: _____

ICS 151
Midterm

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **5 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this midterm are **30 points.**
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

Solution

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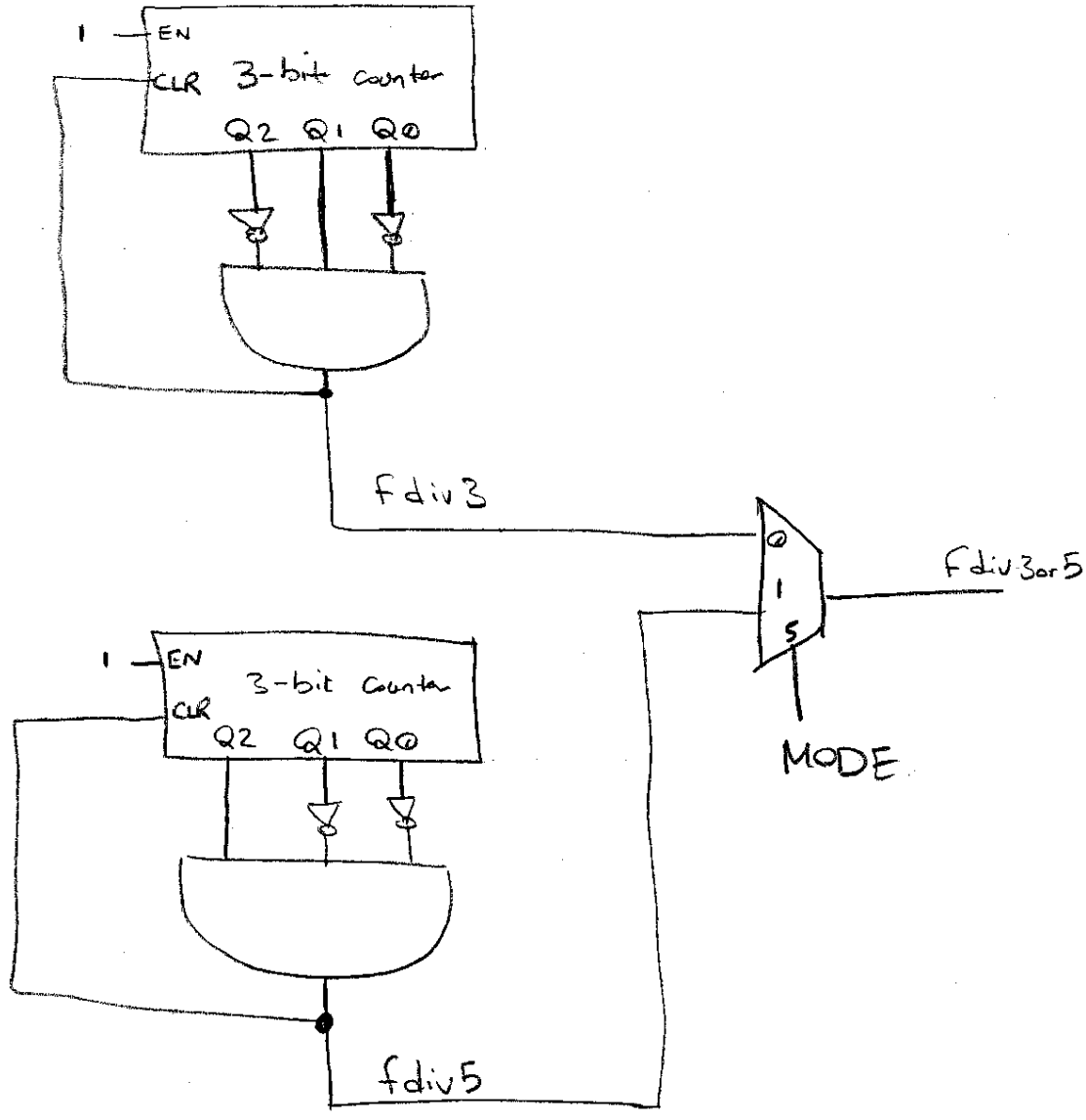
Q1: Circuit Design [20 points]

We want to design a **frequency divider** circuit that divides a given frequency by 3 or 5. If the input MODE=0 it divides the frequency by 3 and if MODE= 1 it divides the frequency by 5. Use as many of the following as needed in your design:

a- 3-bit counter with clear
b- 2-to-1 multiplexer
c- Logic gates (AND, OR, NOT)

Hint: Use mod-3 and mod-5 counters.

First Method



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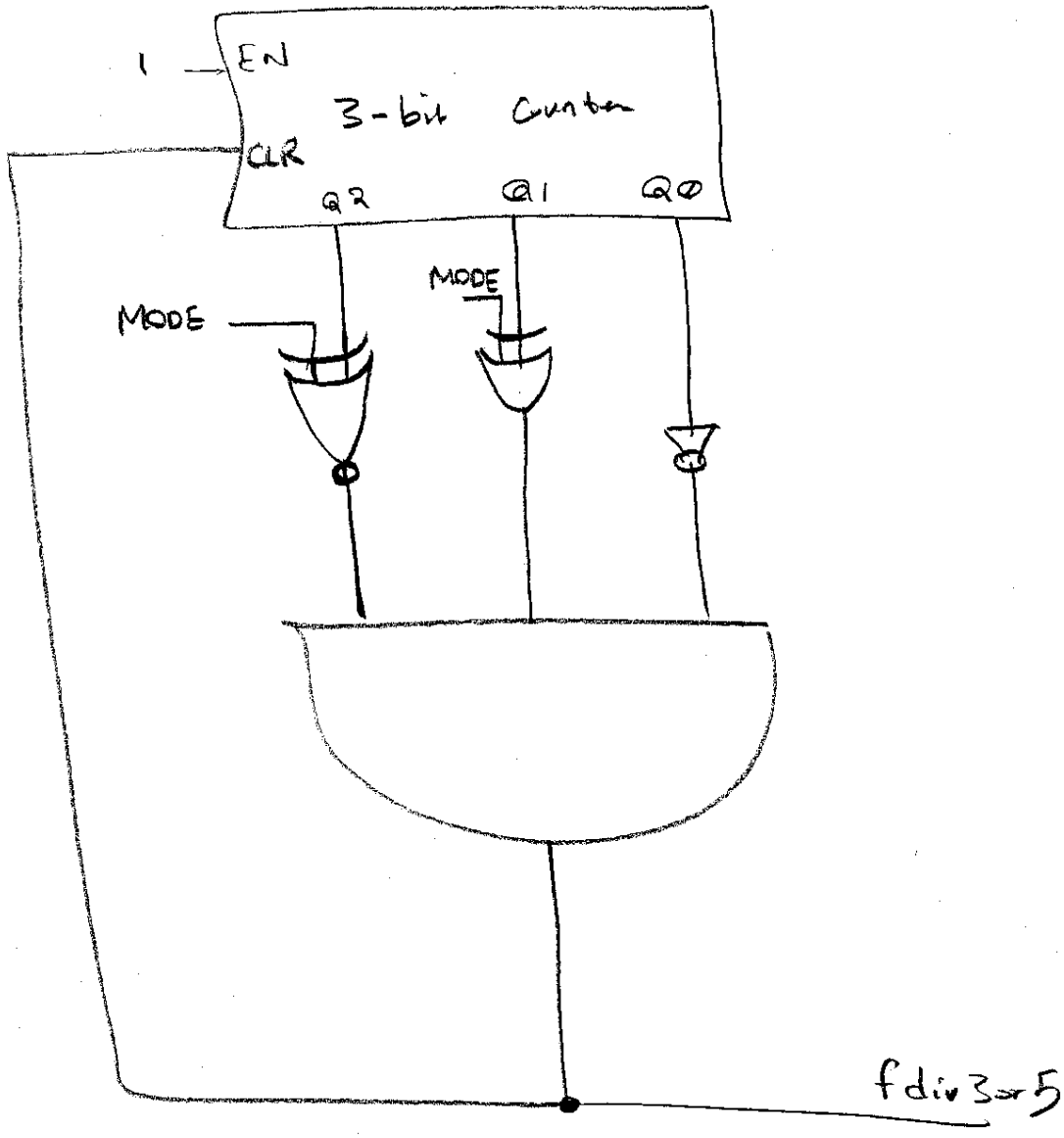
Second Method

$x \oplus 0 = x$

$x \oplus 1 = \overline{x}$



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Q2: Overflow detector for 2's complement [10 points]

We want to add two n-bit 2's complement numbers A and B which has the following forms:

$A = a_{n-1}a_{n-2}\ldots a_0$
$B = b_{n-1}b_{n-2}\ldots b_0$

Let's call the carry out of the $(n-2)^{nd}$ stage, $\mathbf{c_{n-1}}$; the carry out of the the $(n-1)^{st}$ stage, $\mathbf{c_n}$ and $(n-1)^{st}$ bit of sum as $\mathbf{s_{n-1}}$.

a – Complete the following table (**'Overflow'** output shows that overflow happened):

Input			Output		
a_{n-1}	b_{n-1}	c_{n-1}	c_n	s_{n-1}	Overflow
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

b- Express the Overflow condition in term of $\mathbf{c_n}$ and $\mathbf{c_{n-1}}$ only. (Note that this is another method for deriving the 2's complement overflow condition).

$$Overflow = c_{n-1} \cdot \overline{c_n} + \overline{c_{n-1}} \cdot c_n$$

$$= c_{n-1} \oplus c_n$$