ICS143A: Principles of Operating Systems

Lecture 12: Interrupts and Exceptions (part 2)

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Privilege levels again
Started boot: no CPL yet
Prepare to load GDT entry #1

**GDT**
- NULL: 0x0
- KCODE: DPL=0, 0 - 4GB
- KDATA: DPL=0, 0 - 4GB
- K_CPU: DPL=0, 4 bytes
- CODE: DPL=3, 0 - 4GB
- DATA: DPL=3, 0 - 4GB
- TSS: sizeof(ts)

```plaintext
ljmp 1, $start32
```

**CPU Register Diagram**
- CS: EIP:
- SS: ESP:
- GDT: gdt TSS:
- IDT: idt CR3:
- CR0:
- CR1:
- CR2:
- CR3:
- CR4:
Privilege levels

- Each segment has a privilege level
  - DPL (descriptor privilege level)
  - 4 privilege levels ranging 0-3
Now CPL=0. We run in the kernel.
iret: return to user, load GDT #4
Run in user, CPL=3
Privilege levels

• Currently running code also has a privilege level
  • “Current privilege level” (CPL): 0-3
  • It is saved in the %cs register
Privilege level transitions

- CPL can access only less privileged segments
  - E.g., 0 can access 1, 2, 3
- Some instructions are “privileged”
  - Can only be invoked at CPL = 0
  - Examples:
    - Load GDT
    - MOV <control register>
      - E.g. reload a page table by changing CR3
Real world

- Only two privilege levels are used in modern OSes:
  - OS kernel runs at 0
  - User code runs at 3
- This is called “flat” segment model
  - Segments for both 0 and 3 cover entire address space
- But then... how the kernel is protected?
Page table: user bit

- Each entry (both Level 1 and Level 2) has a bit
  - If set, code at privilege level 3 can access
  - If not, only levels 0-2 can access
- Note, only 2 levels, not 4 like with segments
- All kernel code is mapped with the user bit clear
  - This protects user-level code from accessing the kernel
Back to interrupts
Recap: interrupt path, no PL change
Processing of interrupt (cross PL)

• Assume we're at CPL =3 (user)
Interrupt descriptor

- Interrupt is allowed
  - If current privilege level (CPL) is less or equal to descriptor privilege level (DPL)
- The kernel protects device interrupts from user
Interrupt descriptor

- Note that this new segment can be more privileged
  - E.g., CPL = 3, DPL = 3, new segment can be PL = 0
  - This is how user-code (PL=3) transitions into kernel (PL=0)
Stack

- Can we continue on the same stack?
Stack

- But how hardware knows where it is?
TSS: Task State Segment (yet another table)

User stack of a process (can grow up to 2GBs)

Interrupt Vector #

Timer: IRQ0 -> vector 32

Kernel Stack of a process (4K)

Code, data, heap

Process

Argument 1
Argument 2
Calling EIP ++
Old EBP
Local variables
Saved local values, e.g. push EAX, etc

EBP →

Last stack frame

Kernel code

vector32

Page table
Level 1

Level 2

GDT

IDT

TSS

CS : #1
SS : #2
GDT: gdt
IDT: idt
EIP: <kernel>
ESP: <kernel>
TSS: tss
CR3: pt

K_CODE: 0 - 4GB
K_DATA: 0 - 4GB
K_CPU: 4 bytes
CODE: 0 - 4GB
DATA: 0 - 4GB
TSS: sizeof(ts)

NULL: 0x8
...
Task State Segment

- Another magic control block
  - Pointed to by special task register (TR)
- Lots of fields for rarely-used features
- A feature we care about in a modern OS:
  - Location of kernel stack (fields SS/ESP)
    - Stack segment selector
    - Location of the stack in that segment
Processing of interrupt (cross PL)

1. Save ESP and SS in a CPU-internal register

2. Load SS and ESP from TSS

3. Push user SS, user ESP, user EFLAGS, user CS, user EIP onto new stack (kernel stack)

4. Set CS and EIP from IDT descriptor's segment selector and offset

5. If the call is through an interrupt gate clear some EFLAGS bits

6. Begin execution of a handler
Stack Usage with Privilege-Level Change

Interrupted Procedure’s Stack

ESP Before Transfer to Handler

Handler’s Stack

SS
ESP
EFLAGS
CS
EIP
Error Code

ESP After Transfer to Handler
Complete interrupt path

User state (saved by hardware)
- SS
- ESP
- EFLAGS
- CS
- EIP

Kernel Stack of a process (4K)

User stack of a process (can grow up to 2GBs)

Page table
- Level 1
- Level 2

Timer: IRQ0 -> vector 32

Interrupt Vector #

Kernel code
Return from an interrupt

• Starts with IRET

1. Restore the CS and EIP registers to their values prior to the interrupt or exception
2. Restore EFLAGS
3. Restore SS and ESP to their values prior to interrupt
   - This results in a stack switch
4. Resume execution of interrupted procedure
x86 interrupt table

Device IRQs

Reserved for the CPU

Software Configurable
Interrupts

- Each type of interrupt is assigned an index from 0—255.
  - 0—31 are for processor interrupts fixed by Intel
  - E.g., 14 is always for page faults
- 32—255 are software configured
  - 32—47 are often for device interrupts (IRQs)
  - Most device’s IRQ line can be configured
- Look up APICs for more info (Ch 4 of Bovet and Cesati)
- 0x80 issues system call in Linux (more on this later)
Sources

• Interrupts
  • External
    – From a device
    – Through CPU pins connected to APIC
  • Software generated with INT n instruction

• Exceptions
  • Processor generated, when CPU detects an error in the program
    – Fault, trap, abort
  • Software generated with INTO, INT 3, BOUND
Software interrupts

- The INT n instruction allows software to raise an interrupt
  - 0x80 is just a Linux convention
  - You could change it to use 0x81!
- There are a lot of spare indexes

- OS sets ring level required to raise an interrupt
  - Generally, user programs can’t issue an int 14 (page fault manually)
  - An unauthorized int instruction causes a general protection fault
    - Interrupt 13
Disabling interrupts

- Delivery of maskable interrupts can be disabled with IF (interrupt flag) in EFLAGS register

- Exceptions
  - Non-maskable interrupts (see next slide)
  - INT n – cannot be masked as it is synchronous
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<th>Mnemonic</th>
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<td>Divide Error</td>
<td>DIV and IDIV instructions.</td>
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<td>#DB</td>
<td>Debug</td>
<td>Any code or data reference.</td>
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<td>#NP</td>
<td>NMI Interrupt</td>
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<td>#UD</td>
<td>Invalid Opcode (UnDefined Opcode)</td>
<td>UD2 instruction or reserved opcode.</td>
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<td>Device Not Available (No Math Coprocessor)</td>
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2. Floating-point instruction.
3. Any data reference in memory.
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Nonmaskable interrupts (NMI)

- Delivered even if IF is clear, e.g. interrupts disabled
  - CPU blocks subsequent NMI interrupts until IRET

- Sources
  - External hardware asserts the NMI pin
  - Processor receives a message on the system bus, or the APIC serial bus with NMI delivery mode

- Delivered via vector #2
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