

Aseem Gupta

Austin, TX 78759

Cell: (949)-232-7349
aseem.gupta@freescale.com

Summary

Highlights:

- Research on temperature-aware VLSI design for low power, improved reliability, & manufacturability.
- Research resulted in more than 20 publications, 2 patent applications & mention in EE Times article.
- Industrial experience with various stages of VLSI design, negotiations, contracts, evaluation of business plans, operations decision management, & product marketing.
- Courses on marketing, negotiations, business law, & entrepreneurship at business management school.

Education

Ph.D. in Embedded Computer Systems June, 2009
University of California, Irvine GPA: 3.937/4.0

Research Area: Low Power and Thermal-Aware Design Techniques
Research supported by Semiconductor Research Corporation (SRC)

Master of Science in Computer Engineering August, 2004
The University of Arizona, Tucson GPA: 3.857/4.0

Bachelor of Electrical Engineering 2002
Madhav Institute of Technology & Science, India 1st Class, Distinction: 83.3%

Business Courses at University of California Irvine

Marketing Strategies for Hi-Tech Companies

- Focus on marketing of technology products, technical uncertainty, technology licensing strategies, product bundling, usage-based pricing, compatibility issues, product line design, competition management.
- Projects on marketing strategies of NVIDIA-EVGA and Meggitt.

Marketing

- Focus on developing coherent marketing strategies, product positioning, pricing, distribution, promotion & market research for existing and new products. Attended classes with express consent of the instructor.

Entrepreneurship & Business Plans

- Graduate course on entrepreneurship and business plan development.
- Developed a business plan which received *top grade* based on instructor review and peer votes.
- The course facilitated interaction with entrepreneurs and venture capitalists.

Negotiations

- Course focused on developing analytical & interpersonal skills for business negotiations.
- Involved interactive hands-on negotiation exercises and scenario simulations.

Business Law

- Course on corporate law which focussed on general contracts, UCC governed sales contracts, negotiable instruments, secured transactions, business organization, and SEC rules.
- Ranked among *top four* out of fifty six students. Scored *100%* marks on the comprehensive final exam.

Professional Experience

Freescale Semiconductor Inc., Austin, TX

July'09 - present

- Working with the EDA tools and Strategy group.
- Responsible for introducing thermal awareness to different steps of physical design flow.

Freescale Semiconductor Inc., Austin, TX

July'05 - Feb'06, June'07 - Sep'07, June'08 - Sep'08

- Proposed & developed thermal-aware floorplanners for reducing leakage power & enhancing reliability.
- Proposed thermal-aware cell V_t optimization & design rule check (DRC) for manufacturability (DFM).
- Did thermal and power analysis of 65nm designs using internal thermal analysis tools.
- Worked with the contracts & negotiations team in the SoC ecosystem enablement group.

Season Rotogravure Pvt. Ltd., India

March'08 - April'09

- Evaluated business plans for feasibility, 3-year revenue projections, market scope and competition.
- Played active role in the decision process for selection and configuration of multiple manufacturing lines.
- Assisted in negotiations on agreements aggregating to the tune of \$1 Million.
- Responsibilities included formulating near-term and long-term marketing strategies, customer discrimination policies, new product placement, competition management, and creation of sales channels.

University of California, Irvine, CA

Jan'05 - June'09

My research interests were in several areas: • Temperature-aware leakage estimation & optimization

- Communication architecture (bus) based dynamic thermal management and memory power reduction
- Thermal-aware SRAM design for reliability and low power
- Register file thermal management by regionalizing and access pattern redistribution
- Dynamic power & thermal management in SMT processors at microarchitectural level
- Temperature-aware global routing & interconnect design
- Modeling in SpecC (C based) & SystemC (C++ based) system description languages

The University of Arizona, Tucson, AZ

Jan'03 - Aug'04

- Worked with Prof. Jerzy Rozenblit on developing a new clustering algorithms and achieved low error rate with outliers.

Zonge Engineering & Research Organization, Tucson, AZ

June'03 - Aug'03

- Developed embedded software for PIC17C756A microcontroller for geophysical survey equipment.

Patents

- [1] Aseem Gupta, Nikil Dutt & Fadi Kurdahi, "Arbiter Driven SRAM Leakage Power Reduction in Bus-Based SoCs," USPTO Application #: 61086768. Assignee: University of California Irvine.
- [2] Aseem Gupta, Puneet Sharma, Kamal Khouri & Magdy Abadir, "Thermal Aware Cell Threshold Voltage Optimization," USPTO Application #: 12/196730. Assignee: Freescale Semiconductor Inc.

Talks & Honors

- [1] Research resulted in over 20 industry & research articles and 2 patent applications.
- [2] Talk at Semiconductor Research Corporation meeting, Stanford University, March'09.
- [3] Participated in the 2009 Paul Merage Business School's Business Plan Competition.
- [4] Talks at Semiconductor Research Corporation - Dallas, Texas Instruments - Dallas, Fujitsu Research Labs - Japan, CODES+ISSS - South Korea, ASP DAC - Japan, ECBS - Czech Republic, ISQED - San Francisco, DATE - France, VLSID - India.
- [5] First prize at the intern poster presentation competition at Freescale Semiconductor Inc, '06.
- [6] Review service for many VLSI - EDA conferences and journals.
- [7] Research mentioned in EE-Times Article "Chip designers feel the heat," 19 June'06.

Publications

- [1] Aseem Gupta, Amin Khajeh, Ahmed Eltawil, Fadi Kurdahi & Nikil Dutt, "RELIEF: Floorplanning for Reliability Improvement in the Presence of Process Variation and Thermal Effects," *Submitted to Asia & South Pacific Design Automation Conference (ASP-DAC)*, 2010.
- [2] Houman Homayoun, Aseem Gupta, Alex Veidenbaum, Fadi Kurdahi & Nikil Dutt, "RAP-RED: Register File Access Pattern Redistribution Mechanism for Power and Thermal Management," *Submitted to Asia & South Pacific Design Automation Conference (ASP-DAC)*, 2010.
- [3] Aseem Gupta, "Temperature Aware VLSI Design for Reduced Power and Reliability Enhancement," *SIGDA Ph.D. Forum at Design Automation Conference*, 2009.
- [4] Aseem Gupta, Sudeep Pasricha, Nikil Dutt, Fadi Kurdahi, Kamal Khouri & Magdy Abadir, "CBTM: Communication Architecture Based Thermal Management for Systems on Chips," *International Symposium of VLSI Design, Automation & Test*, 2009.
- [5] Amin Khajeh, Aseem Gupta, Nikil Dutt, Fadi Kurdahi & Ahmed Eltawil, "TEAM: Temperature and Reliability Aware Memory Design," *Design, Automation & Test Conference (DATE)*, 2009.
- [6] Houman Homayoun, Mohammad Makhzan, Aseem Gupta, Alex Veidenbaum, Nikil Dutt & Fadi Kurdahi, "Lethargic Peripherals: A Circuit/Architectural Technique for Leakage Management in On-Chip SRAM Memories," *Submitted to International Symposium on High-Performance Computer Architecture*, 2009.
- [7] Aseem Gupta, Amin Djahromi, Fadi Kurdahi, Ahmed Eltawil & Nikil Dutt, "Managing Leakage Power and Reliability in Hot Chips Using System Floorplanning and SRAM Design," *International Workshop on Thermal Investigations of ICs and Systems*, 2008.
- [8] Aseem Gupta, Nikil Dutt, Fadi Kurdahi, Kamal Khouri & Magdy Abadir, "System Level Temperature Aware Leakage Power Estimation and Floorplanning for Reduced Leakage Power," *Submitted to IEEE Transactions on VLSI Systems*, 2009, in review.
- [9] Aseem Gupta, Nikil Dutt, Fadi Kurdahi, Kamal Khouri & Magdy Abadir, "Temperature Aware SoC Design for Reduced Leakage Power and Enhanced Reliability," *SRC Techcon Conference*, 2008.
- [10] Aseem Gupta, Nikil Dutt, Fadi Kurdahi, Kamal Khouri & Magdy Abadir, "Thermal Aware Global Routing of VLSI Chips for Enhanced Reliability," *International Symposium of Quality Electronic Design (ISQED)*, 2008.
- [11] Deepa Kannan, Aseem Gupta, Aviral Shrivastava, Fadi Kurdahi, & Nikil Dutt, "PTSMT: A Tool for Cross-Level Power, Performance, and Thermal Exploration of SMT Processors," *International Conference of VLSI Design*, 2008.
- [12] Aseem Gupta, Nikil Dutt, Fadi Kurdahi, Kamal Khouri & Magdy Abadir, "LEAF: A system level leakage aware floorplanner," *Asia & South Pacific Design Automation Conference (ASP-DAC)*, 2007.
- [13] Aseem Gupta, Nikil Dutt, Fadi Kurdahi, Kamal Khouri & Magdy Abadir, "STEFAL: A system level temperature- and floorplan- aware leakage power estimator for SoCs," *International Conference of VLSI Design*, 2007.
- [14] Aseem Gupta, Nikil Dutt, Fadi Kurdahi, Kamal Khouri & Magdy Abadir, "Floorplan driven leakage power aware IP-based SoC design space exploration," *International Conference on Hardware-Software Codesign & System Synthesis (CODES+ISSS)*, 2006.
- [15] Brian Kahne, Aseem Gupta, Peter Wilson & Nikil Dutt, "An introduction to the plasma language," *International Workshop on Microprocessor Test and Verification (MTV)*, 2005.
- [16] Aseem Gupta & Rainer Dömer, "System design of digital camera using SpecC," *Center for Embedded Computer Systems, UCI, Technical Report 04-32*, 2004.

- [17] Claudio Talarico, Aseem Gupta, Ebenzer Peter & Jerzy Rozenblit, "Embedded system engineering using C/C++ based design methodologies," *Conference on Engineering of Computer-Based Systems (IEEE-ECBS)*, 2005.
- [18] Claudio Talarico, Jerzy Rozenblit, Aseem Gupta & Ebenzer Peter, "Performance analysis of embedded systems with SystemC," *Conference on Computing, Communications and Control Technologies (CCCT)*, 2004, invited paper.
- [19] Parul Garg, Aseem Gupta & Jerzy Rozenblit, "Performance analysis of embedded systems in virtual component co-design environment," *Conference on engineering of computer-based systems (IEEE-ECBS)*, 2004.

Other Articles

- [20] Aseem Gupta, Kamal Khouri & Magdy Abadir, "Thermal Aware Variable Sizing of Interconnects," *IP.com Prior Art Database - IPCOM000172864D*, 2008.
- [21] Aseem Gupta, Kamal Khouri & Magdy Abadir, "Thermal Aware Design Rule Checking of Chip Layout," *IP.com Prior Art Database - IPCOM000172857D*, 2008.