IWIA'03 Technical Program

Sunday January 26, 2003

17:00-18:00 Registration

Monday January 27, 2003

8:45 Registration
9:00 Opening
9:15 ***Embedded Systems/Low Power***

Do Embedded Processors Benefit from Adaptability?
Toshinori Sato (Kyushu Institute of Technology, Japan Science and Technology Corporation)

A Comparative Analysis of Power and Energy Management Techniques in Real Embedded Applications
Peter Kogge, Arun Rodriguez (Notre Dame), Jeffrey Nankung, Nazeeh Aranki, N. Benny Toomarian (JPL)

Run-Time Power-Performance Scaling of Embedded Microprocessors in Deep Sub-Micron Technologies
Isao Minematsu, Tetsuya Fujimoto, Koichiro Ishibashi. (Semiconductor Technology Academic Research Center

10:30 Coffee Break

10:45 ***Low Power***

Global Critical Path Predictors for Low Power Microprocessors
Akihiro Chiyonobu, Toshinori Sato, Itsujiro Arita. (Kyushu Institute of Technology)

Reducing Memory System Energy in Data Intensive Computations by Software-Controlled On-Chip Memory
Hiroshi Nakamura*, Masaaki Kondo*,**, Motonobu Fujita*, Taisuke Boku*** and Mitsuhisa Sato***
(*The University of Tokyo, **CREST, Japan Science and Technology Corporation, ***University of Tsukuba)

11:35 ***Discussion***

12:15 Lunch (on your own)

1:45 ***Parallel Systems***

Comparing Large-Scale Systems using Application Performance Models
Darren J. Kerbyson, Adolfy Hoisie, Harvey J. Wasserman (Los Alamos National Lab)

Multigrain Parallel Processing on OSCAR CMP
Keiji Kimura* , Takeshi Kodaka* , Motoki Obata*, ** and Hironori Kasahara*, **
(*Waseda University, **Advanced Parallelizing Compiler Project)

A Design Space Analysis of PIM-based Architecture
Thomas Sterling, Ed Upchurch (NASA Jet Propulsion Laboratory, California Institute of Technology)

3:15 Coffee Break

3:30 ***Multi-threading***

A Dual-Length Path-Based Predictor for Thread Prediction
Niko Demus Barli, Luong Dinh Hung, Hideyuki Miura, Shuichi Sakai,Hidehiko Tanaka (The University of Tokyo)

Overview of On-Chip Multi-SMT Processor OChiMuS
Hironori Nakajo, Shoji Kawahara, Masanori Yamato, Norito Kato, Koichi Sasada, Mikiko Sato, Mitaro Namiki (Tokyo University of Agriculture and Technology)

4:20 ***Discussion***

6:00 Reception

Tuesday January 28, 2003

9:30 ***Compilers***

An experimental study of a new exact test for array data dependence
Tetsutaro UEHARA and Yoshitoshi KUNIEDA (Wakayama University)

Unrolling Shape for Out-of-Order Processors
Hiroyuki Sato (The University of Tokyo)

10:20 ***Discussion***

10:50 Coffee Break

11:10 ***Panel-Led Discussion "Future Directions of Processor Architecture"***

12:00 Lunch (on your own)

1:30 ***MP networks***

Design and Evaluation of a Fault-Tolerant Adaptive Router for Parallel Computers
Tsutomu Yoshinaga, Osamu Mitobe, Hiroyuki Hosogoshi, Masahiro Sowa (University of Electro-Communications)

Performance Evaluation of Bandwidth and Global Operations on DIMMnet-1 Prototype
Noboru Tanabe(Toshiba), Yoshihiro Hamada, Akihiro Mitsuhashi, Hironori Nakajo (Tokyo Univ. of Agriculture and Technology), Junji Yamamoto(Hitachi), Hideki Imashiro(Hitachi IT), Tomohiro Kudoh(RWCP), Hideharu Amano(Keio Univ.)

2:20 ***Discussion***

2:50 Coffee Break

3:00 ***Parallelism***

Runtime Architectures for Lazy Partitioning of Sequential Programs
Masahiro YASUGI (Graduate School of Informatics, Kyoto University)

Fast Context Switching by Hierarchical Task Allocation
Kiyofumi Tanaka (Japan Advanced Institute of Science and Technology)

3:50 ***Discussion***

Wednesday January 29, 2003

9:00 ***Memory Hierarchy***

Spec-all: Aggressive Read/Write Access Speculation Method for DSM Systems
Fumihito Furukawa, Kanemitsu Ootsu, Takashi Yokota and Takanobu Baba (Utsunomiya University)

Adaptive Fetch Size Prediction in Data Caches
Alex Veidenbaum, Weiyu Tang, Alex Nicolau (UC Irvine)

10:30 ***Closing***

11:00 ***Business Meeting***