Aviral Shrivastava

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Research Interests

My research interests lie in **Software for Embedded Systems**, particularly at the boundary of embedded **Processor Architectures and Compilers**. My other interests are CAD algorithms and high-level synthesis.

Education

University of California, Irvine	Ph.D. in Embedded Systems	2006
University of California, Irvine	Masters in Computer Systems	2002
Indian Institute of Technology, Delhi	Bachelors in Computer Science	1999

Doctor of Philosophy

Compiler-in-the-Loop Exploration of Embedded Systems
Advisors: Prof. Nikil Dutt (UCI), Prof. Alex Nicolau (UCI), Eugene Earlie (Intel)

Embedded Systems are characterized by strict, multi-dimensional design constraints, e.g. power, performance, time-to-market. To satisfy all design constraints *in-chorus*, *customization* and *cross-dimension trade-offs* are very important. As a result embedded systems employ *light weight* versions of techniques implemented in high-performance processors, and include several design *idiosyncrasies*, e.g., partial register renaming, partial bypassing. Although architects prefer programmable components to achieve faster time-to-market and easy upgradeability; code generation for such *customized* embedded processors is a daunting task. The challenge in developing compilers for embedded processors is not only in developing compiler technology to exploit the *idiosyncratic* design feature, but also to perform the required analysis in the limited resources present in embedded systems.
When the compiler is able to exploit the idiosyncratic design feature, it often has significant impact on the overall system characteristics. In such cases, the compiler effects cannot be ignored while searching for the optimal processor design. Traditionally exploration to find an optimal processor is performed by simulating the same application binary over different processor variations. The variation that fares best on the cost metric is chosen. Compiler effects in such an exploration scheme are typically accounted for, using ad-hoc methods, like hand-tuning the application binary, or scaling the simulation results. Such ad-hoc methods leave much space for errors and are not reliable. My thesis proposes a Compiler-In-the-Loop (CIL) Design Space Exploration (DSE) methodology to systematically include compiler effects in the search for an optimal embedded processor. My dissertation demonstrates the need and usefulness of CIL DSE at several levels of design abstractions: the micro-architecture level, the architecture level, memory level, and at the processor-memory-interface level. CIL DSE results in a more meaningful exploration of design space, and leads to better designs.

Published Software

S2. **PBExplore**: A Framework for Compiler-in-the-Loop Exploration of Partial Bypasses in Pipelined Embedded Processors.
In use by several PhD students at UCI and at other universities.

S1. **EXPRESSION**: A Processor Architecture Description Language (ADL) based Retargetable Compiler-Simulator tool-chain
In use by several PhD students at UCI and at other universities.

Patents

P2. Provisional Patent, rights owned by UC Regents and Intel on "Operation Tables for Scheduling in the presence of Partial Bypassing in processor pipelines," by Aviral Shrivastava, Eugene Earlie, Nikil Dutt, and Alex Nicolau.

P1. Provisional Patent, rights owned by UC Regents and Intel on "Aggregating Processor and Memory Free Times for Energy Reduction," by Aviral Shrivastava, Eugene Earlie, Nikil Dutt, and Alex Nicolau.

Conference Publications

C11. **[DATE 2006]** International Conference on Design Automation and Test in Europe
Automatic Generation of Operation Tables for Fast Exploration of Bypasses in Embedded Processors
Aviral Shrivastava, Sanghyun Park, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek.

C10. **[CASES 2005]** International Conference on Compiler Architecture and Synthesis for Embedded Systems
Compilation Techniques for Energy Reduction in Horizontally Partitioned Cache Architectures
Aviral Shrivastava, Ilya Issenin, and Nikil Dutt.

C9. **[CODES+ISSS 2005]** International Conference on Hardware - Software Codesign and System Synthesis
Aggregating Processor Free Time for Energy Reduction
Aviral Shrivastava, Eugene Earlie**,** Nikil Dutt, and Alex Nicolau.

C8. [TechCon 2005] Semiconductor Research Corporation, TechCon
Compiler-in-the-Loop, ADL-driven Early Architectural Exploration
Aviral Shrivastava, Nikil Dutt, Alex Nicolau, and Eugene Earlie.

C7. **[DATE 2005]** International Conference on Design Automation and Test in Europe
PBExplore: A Framework for Compiler-in-the-Loop Exploration of Partial Bypassing in Embedded Processors
Aviral Shrivastava, Nikil Dutt, Alex Nicolau, and Eugene Earlie

C6. **[CODES+ISSS 2004]** International Conference on Hardware - Software Codesign and System Synthesis
Operation Tables for Scheduling in the Presence of Incomplete Bypassing - Aviral Shrivastava, Eugene Earlie, Nikil Dutt, and Alex Nicolau.

C5. **[ASPDAC 2004]** Asia South-Pacific Design Automation Conference
***E**nergy Efficient Code Generation using rISA*
Aviral Shrivastava and Nikil Dutt.

C4. **[ISSS 2002]** International Symposium on System Synthesis
A Design Space Exploration Framework for Reduced Bit-width Instruction Set Architecture (rISA) Design
Ashok Halambi, Aviral Shrivastava, Partha Biswas, Nikil Dutt, and Alex Nicolau.

C3. **[DATE 2002]** International Conference on Design Automation and Test in Europe
An Efficient Compiler Technique for Code Size Reduction using Reduced Bit-width ISAs
Ashok Halambi, Aviral Shrivastava, Partha Biswas, Nikil Dutt, and Alex Nicolau.

C2. **[SCOPES 2001]** International Workshop on Software and Compilers for Embedded Systems
A Customizable Compiler Framework for Embedded Systems
Ashok Halambi, Aviral Shrivastava, Nikil Dutt, and Alex Nicolau.

C1. **[VLSI 2000]** International Conference on VLSI Design
Hardware-Software Partitioning of Concurrent Sequence Flow Graphs
Aviral Shrivastava, Mohit Kumar, Sanjiv Kapoor, Shashi Kumar, and M. Balakrishnan.

Journal Articles

J4. [**TODAES**] ACM Transactions on Design Automation of Electronic Systems
ADL-driven Software Toolkit Generation for Architectural Exploration of Programmable SOCs
Prabhat Mishra, Aviral Shrivastava, and Nikil Dutt

J3. [**TVLSI**] IEEE Transactions on VLSI
Retargetable Pipeline Hazard Detection for Partially Bypassed Processors
Aviral Shrivastava, Nikil Dutt, Alex Nicolau, and Eugene Earlie

J2. [**TODAES**] ACM Transactions on Design Automation of Electronic Systems
Compilation Framework for Code Size Reduction using Reduced Bit-width ISAs
Aviral Shrivastava, Partha Biswas, Ashok Halambi, Nikil Dutt, and Alex Nicolau

J1. [**TECS**] ACM Transactions on Embedded Computer Systems (In submission)
Energy Reduction by exploiting Horizontally Partitioned Caches
Ilya Issenin, Aviral Shrivastava, and Nikil Dutt

Designs

D1. **[VLSI 1999]** International Conference on VLSI Design
An optimized design of 32-bit Floating Point Multiplier
Aviral Shrivastava and Pankaj Bharti (Poster Presentation)

Recent Talks and Awards

Invited Speaker at OCASA 2005 (Optimizing Compiler-Assisted SoC Assembly Workshop
Spring 2005 Dissertation Fellowship, University of California, Irvine
SRC Funded Student 2003-2005 (Semiconductor Research Corporation)

Teaching Experience

Guest Lecturer, ICS 151: Digital Logic Design, fall 2005
Teaching Assistant, ICS 161: Design and Analysis of Algorithms, spring 2002
Teaching Assistant, ICS 151: Digital Logic Design, 2001

Work Experience

Research Intern, Strategic CAD Labs, Intel Corporation, Hudson, MA, July 2003 – Dec 2003
Research Intern, PICO Group, HP Labs, Palo Alto, CA, July 2002 – Sep 2002
CAD Engineer, Library Technology Group, Nijmegen, Philips Netherlands, Sep 1999 – June 2000
Research Assistant, Computer Science and Engineering, IIT Delhi, India, May 1999 – Aug 1999

References

Prof. Nikil Dutt, University of California, Irvine, dutt@ics.uci.edu
Prof. Alex Nicolau, University of California, Irvine, nicolau@ics.uci.edu
Prof. Tony Givargis, University of California, Irvine, givargis@ics.uci.edu
Eugene Earlie, Strategic CAD Labs, Intel, eugene.earlie@intel.com
Prof. Scott Mahlke, University of Michigan Ann Arbor, mahlke@umich.edu