Solutions for Homework 4

5. Use the table from hw2-1, #1a:

A	B	C	E
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The inputs d1, d2, d4, and d7 of the multiplexer in Fig. 3-12a are set to 1, the rest is set to 0. (Analogous to Fig. 3-12b.)

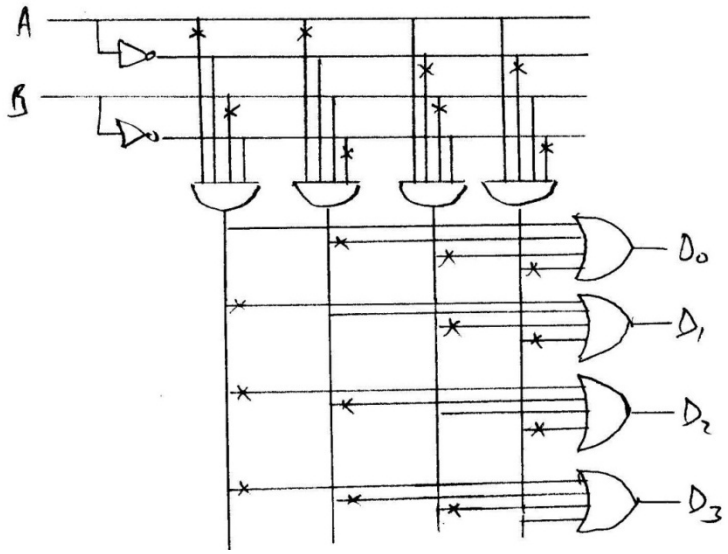
8.

A0	A1	B0	B1	E
0	0	0	0	1
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	1
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	1
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	1

E = A0’A1’B0’B1’ + A0’A1B0’B1 + A0’A1B0’B1 + A0A1B0B1

The diagram has 4 AND gates (with 4 inputs each); the four AND gates are connected to an OR gate. (Analogous to circuit Fig 3-3b, only with 4 inputs A0, A1, B0, B1, instead of A, B, C.)

10.



11. Simply connect a 1 to the one input of the demultiplexer. The 3 control lines ABC are then "decoded" onto the 8 output lines d0-d7. I.e., when ABC=000, d0=1, when ABC=001, d1=1, etc.

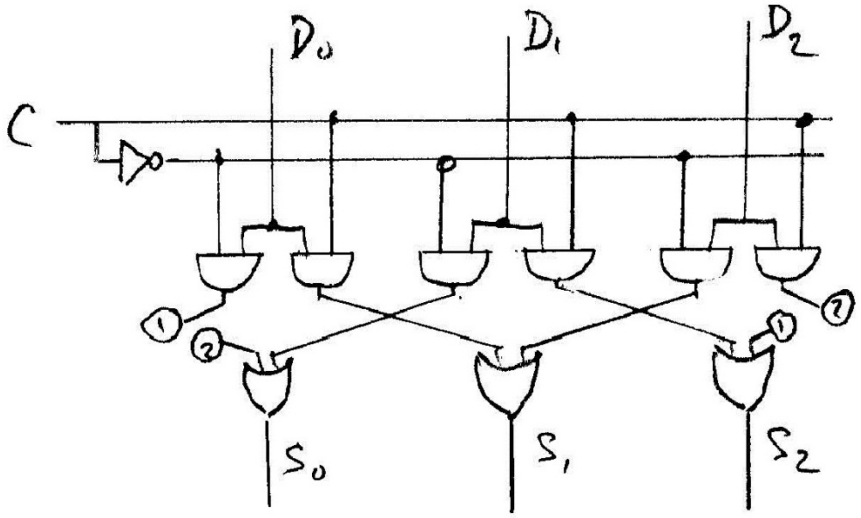
12. The mux has 4 inputs d0-d3 and 2 controls AB, and output.

a. OR gate: connect a 1 to d1, d2, d3. Thus only when AB=00 will the output be 0.

b. XOR: connect a 1 to d1 and d2.

c. NAND: connect a 1 to d0, d1, d2.

13.



16.

F0	F1	ENA	ENB	INVA	Cin	Out	Cout
0	0	1	1	0	0	**1**	**0**
0	0	0	1	1	1	**1**	**0**
1	0	1	1	0	1	**0**	**0**
1	0	0	0	0	0	**1**	**0**
1	1	1	1	0	1	**1**	**1**
1	1	0	1	0	1	**0**	**1**
1	1	1	0	1	1	**1**	**0**
1	1	0	0	0	1	**1**	**0**