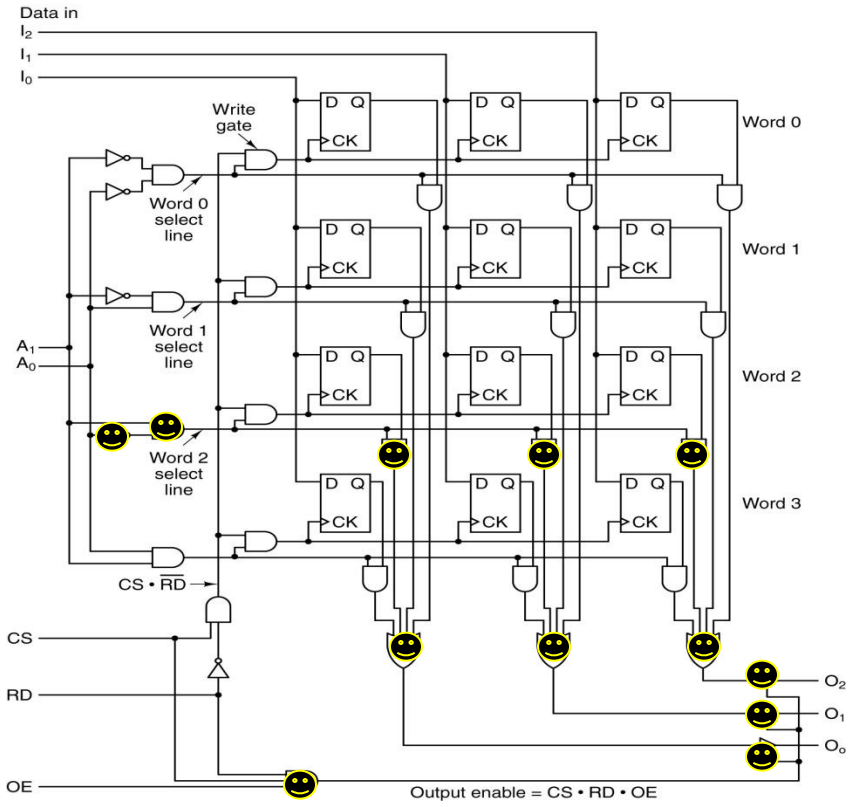
Solutions for Homework 5

19.

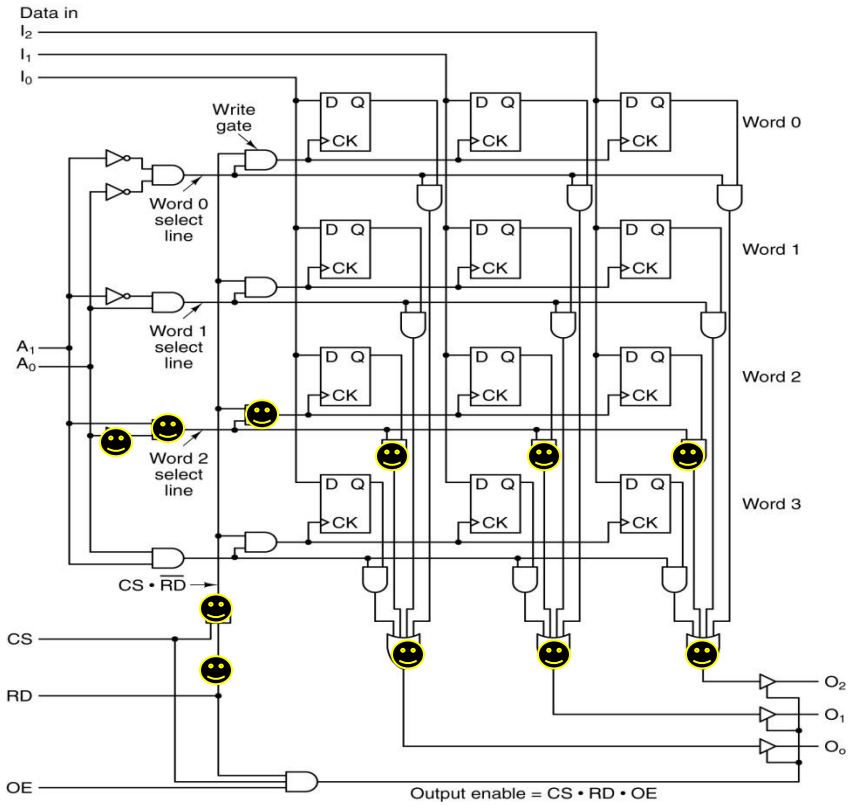
t	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
S	0	1	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1	0
R	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	1	0
Q	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**?**

20.
The design uses two AND gates for chip enable logic plus two AND gates per word select line plus one AND gate per data bit. For a 256 × 8 memory this comes to 2 + 512 + 2048 = 2562 AND gates. The circuit also uses one OR gate for each bit in the word; hence eight of them would be needed.

21. a.



b.



22.
From the midpoint of T1 to the midpoint of T3 it is 40 nsec. So the memory has 40-T_M-T_{DS}=40-3-2=35 nsec to respond.

23.
In regular mode it takes 3 cycles per block, i.e. 3n for n blocks. In block mode it takes 3 for the first block and 1 for each subsequent block, i.e., 3+n-1 = 2+n.
The increase in bandwidth is then 3n/(2+n). For large n this approaches 3, i.e., 3 times as much bandwidth using block transfer.