

NIKIL DUTT
Professor of CS and EECS
University of California, Irvine

Office Address

Department of Computer Science, 444 CS
University of California, Irvine, CA 92697-3425, USA
Tel: +1 (949) 824-7219
Fax: +1 (949) 824-7219
Alternate Fax: +1 (949) 824-8019
Email: dutt@uci.edu
URL: <http://www.ics.uci.edu/~dutt>

Home Address

5 McClintock Court
Irvine, CA 92612-4046, USA
Tel: +1 (949) 856-2473

PERSONAL DATA

Date of Birth: November 9, 1958

Place of Birth: Hubli, India

Citizenship: U.S.A.

AREAS OF RESEARCH

Computer systems design automation, embedded systems CAD, compilation techniques for novel architectures, high-level synthesis and high-level design languages, low-power design, distributed embedded systems.

EDUCATION

- 1989: **Ph.D.** in Computer Science, University of Illinois at Urbana-Champaign.
1983: **M.S.** in Computer Science, The Pennsylvania State University, University Park, PA.
1981: **B.E. (Honors) with Distinction** in Mechanical Engineering, Birla Institute of Technical & Science, (BITS) Pilani, India.

ACADEMIC APPOINTMENTS

- July 2003 – June 2004 : **Vice-Chair**, Division of Computer Systems, Department of Computer Science, U.C. Irvine.
January 2003 - : **Professor**, Department of Computer Science and Department of Electrical Engineering and Computer Science, and **Director**, ACES Laboratory, Center for Embedded Computer Systems, U.C. Irvine
July 1998 – December 2002: **Professor**, Department of Information and Computer Science and Department of Electrical and Computer Engineering and **Director**, ACES Laboratory, Center for Embedded Computer Systems, U.C. Irvine.
July 1997 - June 1998, and July 1999 - June 2000: **Associate Chair of Graduate Studies**, Department of Information and Computer Science, U.C. Irvine.
July 1994 - June 1998: **Associate Professor**, Department of Information and Computer Science and Department of Electrical and Computer Engineering, U.C. Irvine.
April 1990 - June 1994: **Assistant Professor**, Department of Information and Computer Science and Department of Electrical and Computer Engineering, U.C. Irvine.
July 1989 - March 1990: **Assistant Professor**, Department of Information and Computer Science, U.C. Irvine.

Jan. 1989 - June 1989: **Lecturer**, Department of Information and Computer Science, U.C. Irvine.

1983 - 1988: **Research and Teaching Assistant**, Department of Computer Science, University of Illinois at Urbana-Champaign.

1981 - 1983: **Research and Teaching Assistant**, Department of Computer Science, Pennsylvania State University, University Park, PA.

RESEARCH CENTER AFFILIATIONS AT UCI

- Center for Embedded Computer Systems (CECS)
- California Institute for Information Technology and Telecommunications (CAL-IT2)
- Center for Pervasive Communications and Computations (CPCC)

AWARDS AND HONORS

Keynotes and Distinguished Lectures

- **Distinguished Speaker Seminar:** ECE Department at the University of Arizona, Tuscon, AZ, April 2006.
- **Distinguished Lecture:** CSE Department at Arizona State University, Tempe, AZ, October 2005.
- **Distinguished Lecture:** 25th Anniversary of the CSE Department at University of South Florida, Tampa, FL, April 2005.
- **Keynote Speaker:** DSD'2004: 30th EUROMICRO Symposium on Digital System Design: Architectures, Methods, Tools, September 2004.
- **IEEE Computer Society Distinguished Visitor Program**, 2003-2005.
- **"ACM SIGDA Distinguished Lecturer,"** 2001 ACM SIGDA Distinguished Lecturer Series in Asia.

Best Paper Awards

- **"Best Paper Award,"** Asia and South Pacific Design Automation Conference 2006 (ASP-DAC 2006), Yokohama, Japan, January 2006.
- **"Best Paper Award,"** 2006 IEEE Consumer Communications and Networking Conference (CCNC 2006), Las Vegas, NV, January 2006.
- **"Best Paper Award,"** First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis (CODES+ISSS 2003), Newport Beach, CA, October 2003.
- **"A. K. Chowdhary Best Paper Award,"** IEEE/ACM Conference on VLSI Design, New Delhi, January 2003.
- **"Best Paper Award,"** *IEEE/ACM/IFIP Tenth International Symposium on Computer Hardware Description Languages*, Marseille, France, April 1991.
- **"Best Paper Award,"** *IEEE/ACM/IFIP Ninth International Symposium on Computer Hardware Description Languages*, Washington DC, June 1989.

Best Paper Award Nominations

- **"Best Paper Award Candidate,"** 2006 International Conference on VLSI Design, Hyderabad, India, January, 2006.

- **“Best Paper Award Nomination,”** 42nd Design Automation Conference (DAC-2005), Anaheim, CA, June 2005.
- **“Best Paper Award Candidate,”** Third Workshop on Application-Specific Processors (WASP’04), Stockholm, Sweden, September 2004.

Teaching Awards

- **“2001 ICS Teaching Excellence Award,”** Senate Faculty members, Honorable Mention, University of California at Irvine, May 2001.
- **“Faculty Recognition Award for Excellence in Teaching,”** Associated Students of the University of California at Irvine (ASUCI), June 1997.
- **“Excellence in Undergraduate Teaching Award,”** The Division of Undergraduate Studies, The Instructional Resources Center and The Committee on Teaching Quality, University of California at Irvine, 1996-1997.
- **“Outstanding Teaching Assistant Award,”** University of Illinois at Urbana-Champaign, Spring 1986.

Professional Service Awards

- **“Special Service Award,”** For Outstanding Service on the ICCAD Executive Committee, 2004-2005.
- **“ACM SIGDA Service Award,”** In Appreciation of Contributions to ACM/SIGDA, June 2005.
- **“ACM Recognition of Service Award,”** In Appreciation of Contributions to the Association for Computing Machinery (ACM) for service as SIGDA Vice Chair, July 1 1999 - June 30, 2001.
- **“ACM Recognition of Service Award,”** In Appreciation of Contributions to the Association for Computing Machinery (ACM) for the SIGDA University Booth, July 1, 1993 - June 30, 1997.

Other Awards

- **“Assistant Professor Recognition,”** Rockwell International Corporation, August 1989.
- **“NSF Research Initiation Award,”** 1990 -1992.
- **“IEEE/Air Force Engineering Foundation Research Initiation Grant Offer,”** September 1990 (*declined since I was also awarded an NSF Research Initiation Award*)
- **“ACM SIGDA Honorable Mention Scholarship Award,”** 27th IEEE/ACM Design Automation Conference, Orlando, FL, June 1990.
- Thesis advisor for Prabhat Mishra, **Winner of 2004 EDAA Outstanding Dissertation Award**

PATENTS

PT1 Provisional Patent Disclosure: Dynamic High Level Synthesis of Digital Circuits with Presynthesis Parallelization of Code, with R. Gupta, S. Gupta, and A. Nicolau, filed February 2004. **Full Patent Disclosure filed February 2005.**

PT2 Provisional Patent Disclosure: Systems and Methods for Simulating Instruction Set Architectures, with M. Reshadi, filed May 2004. **Full Patent Disclosure in progress.**

PT3 Provisional Patent Disclosure: Pipeline Hazard Detection Mechanism in Retargetable Compilers with Partial Bypassing, with A. Shrivastava, A. Nicolau, and E. Earlie, filed September 2004.

PT4 Provisional Patent Disclosure: Functional Coverage Driven Test Generation for Validation of Pipelined Processors, with P.Mishra, filed September 2004.

PT5 Provisional Patent Disclosure: Efficient Transaction-based Modeling w/ Cycle Count Accurate at Transaction Boundary (CCATB) Models, with S. Pasricha and M. BenRomdhane, filed December 2004. **Full Patent Disclosure in progress.**

SIGNIFICANT PROFESSIONAL SERVICE

Advisory Boards

July 1993 - present: **Advisory Board Member**, ACM SIGDA.

July 2003 – October 2005: **Advisory Board Member**, ACM SIGBED.

Oct. 2003 - present: **Advisory Board Member**, Center for Embedded Systems for Critical Applications (CESCA), Virginia Tech.

Dec. 1999 – Dec. 2002: **Member**, Technical Advisory Board, Axys Design Automation, Irvine, CA.

Offices Held

- Advisory Board, ACM-SIGDA, 2001-
- Advisory Board, ACM SIGBED, 2003-2005
- Advisory Board, Center for Embedded Systems for Critical Applications, Virginia Tech, 2003-
- Information Director, ACM Special Interest Group on Design Automation (SIGDA), 1998 -2001.
- Vice-Chair, ACM Special Interest Group on Design Automation (SIGDA), 1997 - 2001.
- Vice-Chair, IFIP WG 10.5 on Integrated Electronic Systems Design, 1994 - .
- Elected Senior Member of the IEEE, December 1996.
- Advisory Board: ACM-SIGDA (University Booth Program), 1993 - 1998.
- Elected Member: IFIP WG 10.2 on System Description and Design Tools, 1991 - .
- Kernel Group Member: IFIP Special Interest Group on VHDL (SIG-VHDL), 1994 - .

Editorial Activity

- **Editor-in-Chief**, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, July 2004 –
- **Associate Editor**, *ACM Transactions on Embedded Computer Systems (TECS)*, September 2003 -.
- **Associate Editor**, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, November 1998 – July 2004.
- **Associate Editor**, *Journal of Embedded Computing (JEC)* , Cambridge Scientific Press, 2003- .
- **Guest Editor**, *IEEE Transactions on VLSI Systems (T-VLSI) Special Issue on System-Level Synthesis*, 1999.
- **Associate Editor**, *IEEE Transactions on VLSI Systems (T-VLSI)*, January 1999 - 2001 .

Conference Organization (Steering, Organizing, Executive, Advisory Committee)

- Steering Committee: ACM/IEEE Sixth International Symposium on High Level Synthesis, Dana Point, CA, November 1992.
- Tutorial Organizer: “High-Level Chip and System Synthesis,” IEEE Asia-Pacific Conference on Circuits and Systems 1992 (APCCAS 92), December 1992.
- Steering Committee: VHDL International Users’ Forum Spring 1994 Conference, San Francisco, April 1994.
- Steering Committee: ACM/IEEE Seventh International Workshop on High Level Synthesis, Niagara-on-the-Lakes, Canada, May 1994.
- Steering Committee: Asia and South Pacific Design Automation Conference 1998 (ASP-DAC ‘98), Yokohama, Japan, February 1998.
- Organizing Committee: 11th International Symposium on System Synthesis (ISSS-98), Hsinchu, Taiwan, December 1998.
- Steering Committee: Asia and South Pacific Design Automation Conference 1999 (ASP-DAC ‘99), Hong Kong, January 1999.
- Steering Committee: 12th International Symposium on System Synthesis (ISSS-99), San Jose, CA, November 1999.
- Steering Committee: Asia and South Pacific Design Automation Conference 2000 (ASP-DAC 2000), Yokohama, Japan, January 2000.
- Tutorial Organizer: Embedded Memories in System Design: Technology, Application, Design and Tools, VLSI Design 2001, Bangalore, India, January 2001.
- Steering Committee: Asia and South Pacific Design Automation Conference 2001 (ASP-DAC 2001), Yokohama, Japan, January 2001.
- Executive Committee: Design, Automation, and Test in Europe 2001 (DATE 2001), Munich, Germany, March 2001.
- Steering Committee: Asia and South Pacific Design Automation Conference 2002 (ASPDAC-2002) and VLSI Design 2002, Bangalore, India, January 2002.
- Steering Committee: Asia and South Pacific Design Automation Conference 2003 (ASP-DAC 2003), Kita-Kyushu, Japan, January 2003.
- Organizing Committee: CODES+ISSS 2003, First ACM/IEEE/IFIP Conference on Hardware/Software Codesign and System Synthesis, Newport Beach, CA October 2003.
- Steering Committee: Asia and South Pacific Design Automation Conference 2004 (ASP-DAC 2004), Yokohama, Japan, January 2004.
- Organizing Committee: CODES+ISSS 2004, Second ACM/IEEE/IFIP Conference on Hardware/Software Codesign and System Synthesis, Stockholm, Sweden, September 2004.
- Advisory Committee: International SoC Design Conference (ISOCC 2004), Seoul, Korea, October 2004.
- Executive Committee: International Conference on Computer-Aided Design 2004 (ICCAD 2004), San Jose, CA, November 2004.
- Steering Committee: Asia and South Pacific Design Automation Conference 2005 (ASP-DAC 2005), Shanghai, China, January 2005.
- Organizing Committee: CODES+ISSS 2005, Third ACM/IEEE/IFIP Conference on Hardware/Software Codesign and System Synthesis, New Jersey, September 2005.

- Executive Committee: International Conference on Computer-Aided Design 2005 (ICCAD 2005), San Jose, CA, November 2005.
- Steering Committee and Tutorial Organizer: Asia and South Pacific Design Automation Conference 2006 (ASP-DAC 2006), Yokohama, Japan, January 2006.
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Conference Chair (General, Technical Program, Topic, Panel, etc.)

- ACM/IEEE Sixth International Workshop on High Level Synthesis, Dana Point, CA, November 1992: *Benchmarks Chair*.
- Coordinator: High Level Synthesis Workshop Electronic Mailing List (1991-1995).
- ACM/IEEE Seventh International Symposium on High Level Synthesis, Niagara-on-the-Lakes, Canada, May 1994: *Benchmarks Chair*.
- VHDL International Users' Forum Spring 1994 Conference, San Francisco, April 1994: *Program Chair*.
- EURODAC-95: European Design Automation Conference, Brighton, U.K., September 1995: *Topic Chair*.
- ED&TC-96: European Design and Test Conference, Paris, France, March 1996: *Topic Chair*.
- IFIP Third Asia Pacific Conference on Hardware Description Languages, Standards and Applications (APCHDL 96), India, January 1996: *General Chair*.
- EURODAC-96: European Design Automation Conference, September 1996: *Topic Chair and Program Committee*.
- EURODAC-97: European Design Automation Conference, September 1997: *Topic Chair*
- EURO-PAR'97, Workshop on Design Automation of Parallel VLSI Circuits, Passau, Germany, August 1997: *Vice Program Chair*.
- DATE-98: Design Automation and Test in Europe, February 1998: *Topic Chair*.
- ISSS-98: 11th International Symposium on System Synthesis, December 1998: *Panels Chair*
- APCHDL'99: IFIP Asia Pacific Conference on Chip Description Languages, Japan, October 1999: *Tutorials Chair*
- DATE-2001: Design Automation and Test in Europe, March, 2001: *Tutorial Co-Chair*.
- ICCAD-2002: International Conference on Computer-Aided Design, San Jose, November 2001: *Topic Chair*.
- DATE-2002: Design Automation and Test in Europe, February 2002: *Topic Chair*.
- DATE-2003: Design Automation and Test in Europe, March 2003: *Topic Chair*.
- ICCAD-2003: International Conference on Computer-Aided Design, San Jose, November 2003: *Topic Chair*.
- ASPDAC-2004: Asia-Pacific Design Automation Conference, January 2004: *Technical Program Co-Chair*.
- RTSS-04: 2004 IEEE Real Time Systems Symposium, Lisbon, December 2004: *Program Chair, Track on Hardware/Software Codesign*.
- VLSI Design/ES 2005: The 18th International Conference on VLSI Design and 4th International Conference on Embedded Systems, Kolkatta, India, January 3-7 2005, *Track Co-Chair for Embedded Systems, and Program Committee*.
- DATE-2005: Design Automation and Test in Europe, March 2006: *Topic Chair*.

- ISLPED'06: International Symposium on Low-Power Electronics and Design, October 2006: *Topic Chair for Software and Systems Track*.
- CODES+ISSS 2007: ACM/IEEE/IFIP Conference on Hardware/Software Codesign and System Synthesis: *Technical Program Chair*.

Conference and Workshop Program Committees

- IFIP Eleventh International Conference on Hardware Description Languages (CHDL 93), Ottawa, Canada, April 1993: *Program Committee*.
- IEEE First Asia Pacific Conference on Hardware Description Languages, Standards and Application, Australia 1993: *Program Committee*.
- IEEE Second Asia Pacific Conference on Hardware Description Languages, Standards and Applications, Japan 1994: *Program Committee*.
- VHDL Forum in Europe (VFE) Spring 1994 Conference, Italy 1994: *Program Committee*.
- EURODAC-94: European Design Automation Conference, Grenoble, France, September 1994: *Program Committee*.
- EDAF-94: IFIP 10.2 Working Conference on Electronic Design Frameworks, Brazil, November 1994: *Program Committee*.
- ICCAD-94: International Conference on Computer-Aided Design, Santa Clara, CA 1994: *Program Committee*.
- VHDL Forum in Europe (VFE) Fall 1994 Conference, France 1994: *Program Committee*.
- VHDL Forum in Europe (VFE) Spring 1995 Conference, France 1995: *Program Committee*.
- First IFIP/Esprit Workshop on Libraries, Component Modeling, France 1995: *Program Committee*.
- IFIP Twelfth International Conference on Hardware Description Languages (CHDL 95), Japan, August 1995: *Program Committee*.
- ISSS-95: International Symposium on System Synthesis, Cannes, France, September 1995: *Program Committee*.
- ICVC-95: 4th International Conference on VLSI and CAD, Seoul, Korea, October 1995: *Program Committee*.
- VHDL Forum in Europe (VFE) Spring 1996 Conference, Germany 1996: *Program Committee*.
- DAC-96: The 33rd Design Automation Conference, Las Vegas, NV, July 1996: *Best Paper Award Selection Committee*.
- EUROVHDL-96: European VHDL Conference, September 1996: *Program Committee*.
- ICCAD-96: International Conference on Computer-Aided Design, Santa Clara, CA 1996: *Program Committee*.
- IFIP Thirteenth International Conference on Hardware Description Languages (CHDL 97), Spain, 1997: *Program Committee*.
- Second Workshop on Libraries, Component Modeling and Quality Assurance, Toledo, Spain, April 1997: *Program Committee*.
- 23rd EUROMICRO'97, Design Automation Track: *Program Committee*.
- ISSS-97: 10th International Symposium on System Synthesis, September 1997: *Program Committee*.

- Workshop on Design, Test and Applications (WDTA'98), Dubrovnik, Croatia, June 1998: *Program Committee*.
- Forum on Design Languages (FDL-98), Switzerland, September 1998: *Program Committee*.
- EUROMICRO Workshop on Digital System Design: Architectures, Methods and Tools, Sweden, September 1998: *Program Committee*.
- APCHDL'98: IFIP Fifth Asia Pacific Conference on Hardware Description Languages, Korea, July 1998: *Program Committee*.
- SASIMI'98: Workshop on Synthesis and Simulation of Mixed Technologies, Sendai, Japan, October 1998: *Program Committee*.
- ISSS-98: 11th International Symposium on System Synthesis, December 1998: *Program Committee*.
- DATE-99: Design Automation and Test in Europe, March 1999: *Program Committee*.
- Workshop on Design, Test and Applications (WDTA'99), Dubrovnik, Croatia, June 1999: *Program Committee*.
- EUROMICRO Workshop on Digital System Design: Architectures, Methods and Tools, Milan, Italy September 1999: *Program Committee*.
- Forum on Design Languages (FDL-99), France, September 1999: *Program Committee*.
- APCHDL'99: IFIP Asia Pacific Conference on Chip Description Languages, Japan, October 1999: *Program Committee*.
- ISSS-99: 12th International Symposium on System Synthesis, November 1999: *ICCAD Liaison and Program Committee*.
- DSVV'2000: 2000 International Workshop on Distributed System Validation and Verification (DSVV'2000), Taipei, Taiwan, ROC, April 10-13, 2000: *Program Committee*.
- ICDA2000: International Conference on Chip Design Automation, Beijing, China, August 2000: *Program Committee for APCHDL2000 track*.
- ISSS-2000: 13th International Symposium on System Synthesis, September 2000: *Program Committee*.
- IMS-2000: The 2nd Workshop on Intelligent Memory Systems, in conjunction with ASPLOS-IX, Boston Massachusetts, November 12, 2000: *Program Committee*.
- ISSS-2001: 14th International Symposium on System Synthesis, September 2001: *Program Committee*.
- ICCAD-2001: International Conference on Computer-Aided Design, San Jose, November 2001: *Program Committee*.
- IFIP VLSI-SOC 2001: IFIP International Conference on Very Large Scale Integration, Montpellier, France, December, 2001: *Program Committee*.
- ISSS-2002: 15th International Symposium on System Synthesis, October 2002: *Program Committee*.
- WASP-2002: First Workshop on Application Specific Processors, November 2002: *Program Committee*.
- ASPDAC-2003: Asia-Pacific Design Automation Conference, January 2003: *Program Committee*.
- LCTES-2003: Conference on Languages, Compilers and Tools for Embedded Systems, June 2003: *Program Committee*.
- MDES/RTAS 2003: Workshop on Model Driven Embedded Systems at the Real Time and Applications Symposium, Washington DC, July 2003: *Program Committee*.
- ISLPED'03: International Symposium on Low-Power Electronics and Design, August 2003: *Program Committee*.

- CODES+ISSS 2003: First ACM/IEEE/IFIP Conference on Hardware/Software Codesign and System Synthesis, October 2003: *Program Committee*.
- COLP-03: Workshop on Compilers and Operating Systems for Low Power, held at PACT'03, September 2003: *Program Committee*.
- DSD'2003: EUROMICRO Symposium on Digital System Design: Architectures, Methods, Tools, September 2003: *Program Committee*.
- CTCES 2003: Workshop on Compilers and Tools for Constrained Embedded Systems, Held at CASES-2003, October 2003: *Program Committee*.
- WASP-2003: Second Workshop on Application Specific Processors, December 2003: *Program Committee*.
- IFIP VLSI-SOC 2003: IFIP International Conference on Very Large Scale Integration, December 2003: *Program Committee*.
- DATE-2004: Design Automation and Test in Europe, Feb 2004: *Program Committee*.
- ISLPED'04: International Symposium on Low-Power Electronics and Design, Irvine, August 2004: *Program Committee*.
- DSD'2004: EUROMICRO Symposium on Digital System Design: Architectures, Methods, Tools, September 2004: *Program Committee*.
- HiPC'04: *Program Committee*.
- SCOPES'04: Software and Compilers for Embedded Systems, Amsterdam, September 2004, *Program Committee*.
- CASES'04: Compilers, Architectures and Software for Embedded Systems, Washington DC, September 2004, *Program Committee*.
- MoDES/RTAS 2004: Workshop on Model Driven Embedded Systems at the Real Time and Applications Symposium, Toronto, Canada, July 2004: *Program Committee*.
- CTCES 2004: Workshop on Compilers and Tools for Constrained Embedded Systems, Held at CASES-2004, October 2004: *Program Committee*.
- CODES+ISSS 2004: ACM/IEEE/IFIP Conference on Hardware/Software Codesign and System Synthesis, September 2004: *Program Committee*.
- WASP-2004: Third Workshop on Application Specific Processors, September 2004: *Program Committee*.
- SASIMI-2004: The 12th Workshop on Synthesis And System Integration of Mixed Information Technologies, Kanazawa, Japan, Oct. 2004 *Program Committee*.
- EUC-2004: International Conference on Embedded and Ubiquitous Computing (EUC-04) August 26-28, 2004, Aizu, Japan, *Program Committee*.
- SASIMI-2004: The 12th Workshop on Synthesis And System Integration of Mixed Information Technologies, Kanazawa, Japan, Oct. 2004 *Program Committee*.
- ART-C 2004: Architectures for Real-Time Computing, December 2004: *Program Committee*.
- ICES2004: The First International Conference on Embedded Software and Systems, Zhejiang University, PRC, December 2004: *Program Committee*.
- VLSI Design/ES 2005: The 18th International Conference on VLSI Design and 4th International Conference on Embedded Systems, Kolkatta, India, January 3-7 2005, *Track Co-Chair for Embedded Systems, and Program Committee*.
- RTAS 2005: The 11th IEEE Real-Time and Embedded Technology and Applications, March 2005: *Program Committee*.

- DATE-2005: Design Automation and Test in Europe, March 2005: *Program Committee*.
- IESS2005: The International Embedded System Symposium, Manaus, Brazil, August 2005: *Program Committee*.
- ISLPED'05: International Symposium on Low-Power Electronics and Design, San Diego, August 2005: *Program Committee*.
- DSD'2005: EUROMICRO Symposium on Digital System Design: Architectures, Methods, Tools, September 2005: *Program Committee*
- SBCCI 2005: 18th Symposium on Integrated Circuits and System Design: September 2005: *Program Committee*.
- CODES+ISSS 2005: ACM/IEEE/IFIP Conference on Hardware/Software Codesign and System Synthesis, September 2005: *Program Committee*.
- CASES'05: Compilers, Architectures and Software for Embedded Systems, San Francisco, September 2005, *Program Committee*.
- RTSS-05: 2005 IEEE Real Time Systems Symposium, Miami, FL, December 2005: *Program Committee*.
- EUC-2005: International Conference on Embedded and Ubiquitous Computing (EUC-04) December 6-9, 2005, Nagasaki, Japan, *Program Committee*.
- SASIMI 2006: Workshop on Synthesis and Simulation of Mixed Technologies, Nagoya, Japan, April 2006: *Program Committee*.
- DATE-2006: Design Automation and Test in Europe, March 2006: *Program Committee*.
- RTAS 2006: The 12th IEEE Real-Time and Embedded Technology and Applications, March 2006: *Program Committee*.
- SAMOS VI: Embedded Computer Systems: Architectures, Modeling and Synthesis, July 2005: *Program Committee*.
- DIPES 2006: IFIP Conference on Distributed and Parallel Embedded Systems: *Program Committee*.
- ISLPED'06: International Symposium on Low-Power Electronics and Design, October 2006: *Program Committee*.
- ESTIMEDIA'06: *Program Committee*.
- SBCCI 2006: 19th Symposium on Integrated Circuits and System Design: September 2006: *Program Committee*.
- Low Power Computing Workshop at ICS-2006, Cairns, Australia, July 2006: *Program Committee*.
- RTSS-06: 2006 IEEE Real Time Systems Symposium, Sao Paulo, Brazil, December 2006: *Program Committee*.
- HiPEAC 2007: 2007 International Conference on High Performance Embedded Architectures & Compilers, Ghent, BELGIUM, January 29-30, 2007: *Program Committee*.
- ICFPT'06: IEEE International Conference on Field Programmable Technology December 13-15, 2006, Bangkok Thailand: *Program Committee*.
- LCTES-2007: Conference on Languages, Compilers and Tools for Embedded Systems, June 2007: *Program Committee*.

Strategic Workshops

- Participant: National Science Foundation Workshop on Future Research Directions in CAD for Electronic Systems: "Putting the 'D' Back in CAD", Seattle, WA, May 1996.

- Participant: National Science Foundation Workshop on *New Directions in Compiler Technology*, Anapolis, MD, August 2001.
- Participant: *NSF/SIGDA Embedded Systems Workshop*, Atlanta, GA, Nov. 2001.

Panels

- Panel Statement: “How ‘High’ is High-Level Synthesis?”, *IEEE Computer Society 1992 Workshop on VLSI*, Clearwater Beach, FL, February 2-5, 1992.
- Panel Moderator: “Physical Design Models at the Behavioral Level,” *Focused Workshop on Linking Behavioral and Physical Models of Hardware*, Irvine, CA, May 30, 1992.
- Panel Statement: “Hardware/Software Co-Design: Are there any new problems?”, *IEEE First Asia Pacific Conference on Hardware Description Languages, Standards and Applications*, Australia, December 1993.
- Panel Organizer & Moderator: “Design Reuse: Fact or Fiction?”, *31st ACM/IEEE Design Automation Conference*, San Diego, CA, June 1994.
- Panel Organizer & Moderator: “Impact of Memory Technology and Architectures on System Synthesis,” *International Symposium on System Synthesis (ISSS-97)*, Antwerp, Belgium, September 1997.
- Panel Organizer & Moderator: “If Software is King for Systems-on-Silicon, What’s New in Compilers?” *ICCD-97: International Conference on Computer Design*, Austin, TX, October 1997.
- Panel Organizer: “IP-Based Design: VIP (Very Important Process) or RIP (Rest in Peace)?” *International Symposium on System Synthesis (ISSS-98)*, Hsinchu, Taiwan, December 1998.
- Panel Organizer: “Driving Agenda for Systems Research,” First IEEE/ACM/IFIP Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2003), Newport Beach, October 2003.

Reviewer

Research Proposals :

- NSF (1988 -).
- University of California MICRO (1991 -).
- Board of Regents Research Committee, State of Louisiana (1992).
- California Space Institute, University of California, San Diego (1993).
- NSF SBIR Panel (1995 -).
- NSF CCR/DA Program Review Panel (1999-).
- NSF ITR Program Review Panel (2000-).
- Swedish Research Council (2003)
- Hong Kong Research Council (1997-)
- Australian National Research Council (1998-)
- Canadian National Science and Engineering Research Council (NSERC) (2003-)

Journals :

- Proceedings of the IEEE (1987).
- IEEE Trans. Computer Aided Design of Integrated Circuits and Systems (1989 -).
- IEEE Trans. Circuits and Systems (1991 -).

- IEEE Trans. on VLSI Systems (1992 -).
- IEEE Design and Test of Computers (1991 -).
- Integration, The VLSI Journal (1991 -).
- VLSI Design, (1993).
- Brazilian Journal of Electronics, (1995).
- ACM Trans. on Design Automation of Electronic Systems (1995 -).
- Design Automation for Embedded Systems (1996 -).
- ACM Trans. On Code Optimizations (TACO) (2004-).

Premier Conferences and Workshops :

- IEEE/ACM Design Automation Conference (1987 -).
- IEEE/ACM International Symposium on Computer Architecture (1988 -).
- IEEE International Conference on Computer-Aided Design (1987 -).
- IEEE Custom Integrated Circuits Conference (1987).
- IFIP Applied Formal Methods for Correct VLSI Design (1989).
- IFIP Computer Hardware Description Languages and their Applications (1990 -).
- IEEE/ACM High-Level Synthesis Workshop (1990 -).
- International Computer Symposium (1992).
- International Symposium on VLSI Design (1991 -).
- International Conference on Parallel Processing (ICPP) (1993 -).
- European Conference on Design Automation with EuroVHDL (EURO-DAC) (1992 -).
- European Design Automation Conference (EDAC) (now DATE) (1991-1997).
- Design and Test in Europe Conference (DATE) (1998-).
- Real-Time Systems Symposium (RTSS) (2003-).

Professional Association Memberships

- Senior Member of the IEEE (Computer Society, CAS Society, DATC, TC VLSI, TC Computer Architecture).
- ACM-SIGDA. (Special Interest Group on Design Automation)
- ACM-SIGBED (Special Interest Group on Embedded Systems)
- IFIP WG 10.5.

Ph.D. ADVISEES (Chair)

Pradip Jha,	<i>High-Level Library Mapping for RT Components</i> , October 1995.
Roger Ang,	<i>Library Insertion and Reuse of Datapath Components in High-Level Synthesis</i> , June 1996.
Preeti Panda,	<i>Memory Optimizations and Exploration for Embedded Systems</i> , January 1998.
Peter Grün,	<i>Hardware/Software Memory Customization for Programmable Embedded Systems</i> , Sept. 2001.
Prabhat Mishra,	<i>Specification-driven Validation of Programmable Embedded Systems</i> , March 2004.

(Winner of 2004 EDAA Outstanding Dissertation Award)

Mahesh Naga Mamidipaka, *Power Estimation in High-Performance Memory Structures*, October 2004.
 Partha Biswas *Acceleration beyond Memory Barriers in IS-extensible Processors*, March 2006.
 Aviral Shrivastava *Compiler-in-the-Loop Exploration of Programmable Embedded Systems*, June 2006
 Nick Savoie (co-advisor: Rajesh Gupta)
 Ilya Issenin
 Sudarshan Banerjee
 Sudeep Pasricha
 Kyoungwoo Lee
 Srinivas Bongoni
 Minyoung Kim
 Aseem Gupta
 Luis Angel Bathen
 Jeff Furlong
 Yonghyun Hwang
 Gabor Madl
 Jayram Moornikara

Ph.D. ADVISEES (Committee Member)

Joseph Lis (1991)
 John Roy (1991)
 Allen C-H Wu (1992)
 Elke Rundensteiner (1992)
 James H. Kim (1992)
 Hung Huang (1993)
 Yulin Chen (1993)
 Haigeng Wang (1993)
 Champaka Ramachandran (1994)
 Sanjiv Narayan (1994)
 Frank Vahid (1994)
 Loganath Ramachandran (1994)
 Tsong-Der Har (1994)
 Jie Gong (1995)
 Patrick Murphy (1996)
 Smita Bakshi (1996)
 Steven Wallace (1996)
 Bjarne Hald (*External Ph.D. Examiner at TU Denmark, Lyngby*, 1997)
 Steven Novack (1997)
 Erica Hsiao-Ping Juan (1997)
 Min Xu (1997)
 Chih-Wen Hseuh (1997)
 David Kolson (1998)
 Prasert Kanthamanon (*External Ph.D. Examiner for University of New South Wales*, 1998)
 Fehmina Merchant (1998)
 Jianwen Zhu (1999)
 Nong Fan (2000)
 Hartej Singh (2000)
 Eugene Gendelman (2001)
 Ana Azevedo (2002)
 Sumit Gupta (2003)
 Jong-eun Lee (Seoul National University, 2004)
 Radoslaw Szymanek (*“Opponent” for Ph.D. Examination at Lund University, Sweden*, 2004)
 Weiyu Tang (2004)
 Paolo D’Alberto (2005)
 Jinfeng Liu (2005)
 Dan Nicolaescu (2005)

Efe Yardimci (2006)
Manish Verma (*External Ph.D. Examiner for University of Dortmund, 2006*)
Dexin Li (2006)

Faculty Mentorship Program Advisees

Roger P. Ang, 1993-1994
Rafael Lopez 2003-2004.

M.S. Advisees

Indraneel Ghosh, *High-Level Modeling of Standard Parts in VHDL*, ECE M.S. Thesis, June 1992.
Asheesh Khare, *SIMPRESS: A Simulator Generator Environment for Systems-on-Chip Exploration*, ICS M.S. Thesis, September 1999.
Shannon Tauro, April 2003.
Daniel Massaguer, EECS M.S. Thesis, Winter 2005.

M.S. Advisees (as a Committee Member)

Rajesh Gupta (1990)
Champaka Ramachandran (1990)
Erik Jessen (1991)
Sharon Yu (1992)
David Lee (1992)
Jian Li (1993)
Reynold Leong (1993)
Nirav Dagli (1994)
Lata Ganesan (1995)
Alberto Nannarelli (1995)
Mat Loikkanen (1995)
Joao Lacerda (1996)
Poonam Agrawal (1996)
Zhuzhen Kang (1997)
Hartej Singh (1997)
Wenwei Pan (1997)
Ming-Hau Lee (1997)
Hung-Kang Liu (1997)
Farzad Etemadi (1997)
Yang Zhang (1997)
Joseph J. Balardeta (1998)
Mark Pontius (1998)
Ruiwei Wang (1998)
Tsen-Yi Lin (2001)
Devyani Sharma (2006)

Faculty Visitors Hosted

Sri Parameswaran, University of Queensland, Australia, December 1993 - May 1994.
Hiroshi Nakamura, Tsukuba University, Japan, March 1996 - January 1997.
Hee Seok Kim, Chong Ju University, Korea, August 1996 - August 1997.
Anupam Basu, Indian Institute of Technology, Kharagpur, India, March 1998 - August 1999.
Jong Kwon Chang, Ulsan University, Korea, January 2000 - January 2001.
Frederic Rousseau, University of Grenoble, France, May 2000 - September 2000.
Kitae Hwang, Hansung University, Korea, September 2000 - August 2001.

Kiyoung Choi, Seoul National University, December 2001 – December 2002.
Wonyong Sung, Seoul National University, January 2004-December 2004.
Per Gunnar Kjeldsberg, Norwegian University of Science and Technology, October 2005-June 2006.
Yun-Seok Nam, Korea Poytechnic University, January 2006-December 2006.

Post-Doctoral Scholars Supervised

Dan Brahme, December 1991 - 1993.
Robert Carden, June 1991 - 1993.
Seong Yong Ohm (jointly with F. Kurdahi), September 1993 - September 1995.
Marie-Lise Flottes (jointly with D. Gajski), July 1994 - July 1995.
Hiroyuki Tomiyama, March 1999 - March 2001.
Sumit Gupta, July 2003 – March 2004.
Hyun-Ok Oh, September 2003 – March 2005.
Prabhat Mishra, April 2004-July 2004.

Doctoral Student Visitors Supervised

Jongun Lee, Seoul National University, January 2002 – May 2003.
Sung Hyun Lee, Seoul National University, September 2003 – September 2004.
Jaewon Seo, Korean Advanced Institute of Science and Technology (KAIST), April 2004-April 2005.
Kisun You, Seoul National University, December 2004 – December 2005.
Sanghyun Park, Seoul National University, June-September 2005.
Ameet Patil, January-April 2006.

Industrial Visitors Hosted

Taisei Yoshino, Hitachi Corporation, September 1999 - September 2000.
Yohei Akita, Hitachi Corporation, July 2003 – July 2004.
Qiang Zhu, Fujitsu Laboratories Inc., August 2005-August 2006.

Undergraduate Honor and Research Advisees

David Bainbridge, 1989 - 1990 (ICS Honors Program)
Pat Stephens, 1991 - 1992 (Campus Honors Program)
David DiGrigorio, 1995 - 1998 (ICS & Campus Honors Program)
Steve Ganem, 1997 - 1998 (Campus Honors Program)
Torrey Searle, 1999 - (ICS Honors Program)
Rex Chin-Ju Chen, 2002-2003 (ICS Honors Program)
Robert On, 2002-2003 (ICS Honors Program)
Luis Angel Bathen 2005 (NSF REU Program)
Michael Shimasaki (HSSOE Undergraduate Research Fellow, 2005-2006)
Nicholas Pham (Undergraduate Research Advisee)

Pregraduate Mentorship Program Advisees

Melinda Hardy, 1990 - 1991.

UC LEADS Mentorship Program Advisees

Rafael Lopez, Summer 2001.
Korey Sewell, Summer 2003.

RESEARCH FUNDING

<u>Title</u>	<u>Dates</u>	<u>Agency</u>	<u>Amount</u>
Unrestricted Research Gift	8/06	Hitachi Ltd.	\$50,000
Modeling and Exploiting Cross-Layer Timing in Distributed Embedded Systems (co-PI with Nalini Venkatasubramanian)	7/06-6/07	NSF EHS/CNS	\$125,000
Unrestricted Research Gift	8/05	Fujitsu Ltd.	\$50,000
SOC Power Optimization Framework	7/05-6/08	Semiconductor Research Corp.	\$245,384
SOC Power Optimization Framework	7/05-6/08	CAL-IT2 matching for SRC award	\$38,400
ADL-Driven, Compiler-in-the-Loop Early Microarchitectural Exploration (co-PI with Alex Nicolau)	7/05-6/06	California MICRO/Intel	\$64,938
REU Supplement	6/05-9/05	NSF	\$6,000
ADL-Driven, Compiler-in-the-Loop Early Microarchitectural Exploration (co-PI with Alex Nicolau)	7/04-6/05	California MICRO/Intel	\$59,450
Equipment Donation	4/03-3/04	Xilinx, Inc.	\$18,638
Compiler-in-the-loop ADL-Driven Early Architectural Exploration	9/03-8/06	Semiconductor Research Corp.	\$318,746
Bus-based SOC Architectural Exploration	7/03-6/04	California MICRO/Conexant	\$41,458
ADL-Driven, Compiler-in-the-Loop Early Microarchitectural Exploration (co-PI with Alex Nicolau)	7/03-6/04	California MICRO/Intel	\$78,333
Unrestricted Research Gift	8/02-10/04	Hitachi Ltd.	\$50,000
An Application Development Environment for Complex Heterogeneous Distributed Real-Time Embedded Computing Platforms (co-PI with Alex Nicolau, Rajesh Gupta, Sandeep Shukla, Doug Schmidt)	10/02-9/05	NSF NGS Program	\$460,000
ITR: Virtual Power for the Wireless Campus (co-PI with Michael Franz, Chandra Krintz, Rich Wolinsky, Pai Chou and Tony Givargis)	9/02-8/05	NSF Medium ITR	\$2,000,798
Platform-Oriented CAD for Power and Performance Optimization	7/02-6/05	NSF DA Program	\$96,060
ADL-Based Exploration of Reconfigurable CoProcessors			

	8/02-10/04	Hitachi Ltd.	\$100,000
<i>Coordinated Coarse-grain and Fine-grain Optimizations for High-Level Synthesis</i>	7/02-6/03	California MICRO/Intel	\$82,500
(co-PI with Gupta, Nicolau)			
<i>Background Study and Planning Activity for the National Experimental Platform for Hybrid and Embedded Systems Technology (NEPHEST)</i>	1/02-7/03	DARPA/Lockheed Martin	\$90,641
<i>SRC Master's Fellowship</i>	9/01-8/03	Semiconductor Research Corp.	\$42,964
<i>Feasibility Study for Research in Architecture Description Languages</i>	7/01-6/02	Hitachi Ltd.	\$20,000
<i>Coordinated Coarse-grain and Fine-grain Optimizations for High-Level Synthesis</i>	7/01-6/02	California MICRO	\$75,000
(co-PI with Gupta, Nicolau)			
<i>Unrestricted Research Gift</i>	7/00-6/01	Motorola Corp.	\$500,000
(co-PI with Nicolau)			
<i>Coordinated Coarse-grain and Fine-grain Optimizations for High-Level Synthesis</i>	7/00-6/01	California MICRO	\$78,438
(co-PI with Gupta, Nicolau)			
<i>A Parallelizing Compiler Framework for Integrated System Design</i>	7/00-6/03	Semiconductor Research Corp.	\$450,000
(co-PI with Gupta, Nicolau)			
<i>Unrestricted Research Gift</i>	9/99-8/00	Hitachi Ltd.	\$40,000
<i>Compiler-Controlled Continuous Power-Performance Management (COPPER)</i>	6/00-5/02	DARPA ITO	\$800,790
(co-PI with Nicolau, Veidenbaum, Gupta)			
REU Supplement	1/99-6/99	NSF	\$10,000
NSF Grant	7/97-6/00	NSF	\$389,424
(co-PI with Alex Nicolau)			
Micro	7/97-6/98	California MICRO	\$179,954
(co-PI with Fadi Kurdahi)			
Micro	7/96-6/97	California MICRO	\$179,758
(co-PI with Fadi Kurdahi)			
Research Donation	1/95-12/95	Xilinx Corporation	\$7,925
SRC Grant	7/95-6/96	Semiconductor Research Corp.	\$56,700
Micro	7/95-6/96	California MICRO	\$31,430
(co-PI with Fadi Kurdahi)			
Research Instrumentation	4/95-3/97	NSF	\$71,411
(lead PI)			
SRC Grant	7/94-6/95	Semiconductor Research Corp.	\$62,527
Micro	7/94-6/95	California MICRO	\$27,000

Micro	7/94-6/95	California MICRO	\$40,500
(co-PI with Fadi Kurdahi)			
Research Donation	9/93-8/94	Xilinx Corporation	\$11,495
Micro	7/93-6/94	California MICRO	\$133,420
(co-PI with Fadi Kurdahi)			
SRC Grant	7/93-6/94	Semiconductor Research Corp.	\$62,527
Faculty Research Grant	6/93-6/94	UCI Committee on Research	\$10,000
Minority Student Supplement	12/92-6/93	NSF	\$5,000
SRC Grant	10/92-6/93	Semiconductor Research Corp.	\$48,797
Equipment Donation	3/92	Zycad Corporation	\$50,000
SRC Grant	10/91-9/92	Semiconductor Research Corp.	\$65,246
Micro	10/91-9/92	California MICRO	\$39,344
(co-PI with Dan Gajski)			
SRC Equipment Grant	12/91	Semiconductor Research Corp.	\$28,000
Research Initiation	7/90-6/92	NSF	\$60,000
REU Supplement	7/90-6/92	NSF	\$10,000
SRC Grant	7/90-6/91	Semiconductor Research Corp.	\$59,750
Micro	7/90-6/91	California MICRO	\$114,000
(co-PI with Dan Gajski)			
UCI Research Grant	6/90-6/91	UCI Committee on Research	\$5,000
Faculty Research Grant	4/90-6/90	ICS/UCI	\$3,000
Asst. Prof. Recognition	8/89	Rockwell International	\$18,500
Library and Travel Grants	87-92	ACM SIGDA	\$7,100

PUBLICATIONS

BOOKS

- B1** “High Level Synthesis: Introduction to Chip and System Design,” with D. Gajski, A. Wu and S. Lin, Kluwer Academic Publishers, Norwell, MA, 1992.
Second Printing, Kluwer Academic Publishers, 1993.
- B2** “Memory Issues in Embedded Systems-on-Chip: Optimizations and Exploration,” with P.R. Panda and A. Nicolau, Kluwer Academic Publishers, Norwell, MA, 1998.
- B3** “Memory Architecture Exploration for Programmable Embedded Systems,” with P. Grun and A. Nicolau, Kluwer Academic Publishers, Norwell, MA, 2003, ISBN: 1402073240.
- B4** “SPARK: A Parallelizing Approach to the High-Level Synthesis of Digital Circuits,” with S. Gupta, R. Gupta and A. Nicolau, Kluwer Academic Publishers, Norwell, MA, 2004.
- B5** “Functional Validation of Programmable Embedded Architectures: A Top-Down Approach,” with P. Mishra, Springer-Verlag, 2005.

BOOK CHAPTERS

- BC1** N.D. Dutt and D.D. Gajski, “EXEL: A Language for Interactive Behavioral Synthesis,” *Computer Hardware Description Languages and Their Applications*, J.A. Darringer and F.J. Rammig, Editors, North-Holland 1990 (reprint of paper C3).
- BC2** N.D. Dutt, J. Cho and T. Hadley, “A User Interface for Behavioral VHDL Modeling,” *Computer Hardware Description Languages and Their Applications*, D. Borrione and R. Waxman, Editors, North-Holland 1992 (reprint of paper C7).
- BC3** A. Capitanio, A. Nicolau and N.D. Dutt, “A Hypergraph-Based Model for Port Allocation on VLIW Architectures,” *Massive Parallelism: Hardware, Software and Applications*, M. Mango Furnari, Editor, World Scientific Press 1994, pp. 215-230.
- BC4** P. Conradi and N.D. Dutt, “A Compound Information Model for High-Level Synthesis,” *Electronic Design Automation Frameworks*, F. Rammig and F. Wagner, Editors, Chapman 1995, pp. 189-198.
- BC5** S. Novack, A. Nicolau and N.D. Dutt, “A Unified Code Generation Approach using Mutation Scheduling,” *Code Generation for Embedded Processors*, G. Goossens and P. Marwedel, Editors, Kluwer Academic Publishers 1995, pp. 203-218.
- BC6** C. Ramachandran, P.K. Jha, F. Kurdahi and N.D. Dutt, “Towards Better Accounting of Physical Design Effects in High Level Synthesis,” A. Mignotte and G. Saucier, Editors, Chapman and Hall 1995, pp. 252-258.
- BC7** P. Panda, H. Nakamura, N.D. Dutt and A. Nicolau, “Improving Cache Performance through Tiling and Data Alignment,” in *Solving Irregularly Structured Problems in Parallel*, G. Bilardi, A. Ferreira and J. Rolim, Editors, Springer-Verlag series Lecture Notes in Computer Science (LNCS) 1253, 1997, pp. 167-185.
- BC8** D. Kolson, A. Nicolau and N.D. Dutt, “Copy Elimination for Parallelizing Compilers,” in *Languages and Compilers for Parallel Computing*, S. Chatterjee, J.F. Prins, L. Carter, J. Ferrante, Z. Li, D. Sehr, P.-C. Yew, Editors, Springer-Verlag series Lecture Notes in Computer Science (LNCS) Volume 1656, 1999, pp. 275-289.

- BC9** A Halambi, N.D. Dutt and A. Nicolau, " Customizing Software Toolkits for Embedded System-On-Chip," in *Architecture and Design of Distributed Embedded Systems*, Bernd Kleinjohann, Editor, Kluwer Academic Publishers, 2001, pp. 87-97.
- BC10** P. Grun , N. D. Dutt , A. Nicolau, "Aggressive Memory-Aware Compilation," in *Intelligent Memory Systems*, F.T. Chong, C. Kozyrakis, M. Oskin, Editors, Lecture Notes in Computer Science Publisher: Springer-Verlag Heidelberg ISSN: 0302-9743, Volume 2107 / 2001, pp. 147-151.
- BC11** P. Mishra and N.D. Dutt, "Modeling and Verification of Pipelined Embedded Processors in the Presence of Hazards and Exceptions," in *Design and Analysis of Distributed Embedded Systems*, Bernd Kleinjohann et al., Editors, Kluwer Academic Publishers, 2002, pp. 81-90.
- BC12** Preeti Ranjan Panda, Nikil D. Dutt, "Memory Architectures for Embedded Systems-on-Chip," in *High Performance Computing*, S. Sahni, V.K. Prasanna, U. Shukla, Editors, Lecture Notes in Computer Science (LNCS) Vol. 2552, Springer-Verlag, 2002, pp. 647-662.
- BC13** M. Kandemir and N.D. Dutt, "Memory Systems and Compiler Support for MPSOC Architectures," in *Multiprocessor Systems-on-Chip*, edited by A. Jerraya and W. Wolf, Morgan Kaufmann Publishers, 2004, pp. 251-281..
- BC14** A. Gordon-Ross, C. Zhang, F. Vahid and N.D. Dutt, "Tuning Caches to Applications for Low-Energy Embedded Systems" in *Ultra Low-Power Electronics and Design*, Enrico Macii, Editor, Kluwer Academic Publishers, 2004, pp. 103-122.
- BC15** S. Mohapatra, N. Venkatasubramanian, N.D. Dutt, C. Pereira, and R. Gupta, "Energy-Aware Adaptations for End-to-end Video Streaming to Mobile Handheld Devices," in *Ultra Low-Power Electronics and Design*, Enrico Macii, Editor, Kluwer Academic Publishers, 2004, pp. 255-273.
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- BC16** L. Cheng, S. Bossi, S. Mohapatra, M. El Zarki, N. Venkatasubramanian, and N.D. Dutt, "Quality Adapted Backlight Scaling (QABS) for Video Streaming to Mobile Handheld Devices," in *Networking – ICN 2005: 4th International Conference on Networking*, Editors: Pascal Lorenzo and Petre Dini, Lecture Notes in Computer Science Publisher: Springer-Verlag Heidelberg ISSN: 0302-9743, Volume 3420/2005, pp. 662- 671.
- BC17** P. Mishra and N.D. Dutt, "Processor Modeling and Design Tools," in *EDA Handbook*, Luciano Lavagno, Grant Martin and Lou Scheffer, Editors, CRC Press 2005.
- BC18** P. Mishra and N. Dutt, "Architecture Description Languages for Programmable Embedded Systems," in *System On Chip: Next Generation Electronics*, Bashir M. Al-Hashimi, Editor, IEE Press, 2006, pp. 187-220.
- BC19** P. Mishra and N.D. Dutt, "Architecture Description Languages," in *Customizable and Configurable Embedded Processors*, Paolo Ienne and Rainer Leupers, Editors, Morgan Kaufman, 2006.
- BC20** G. Madl and N. Dutt, "Domain-specific Modeling of Power Aware Distributed Real-time Embedded Systems", SAMOS VI: Embedded Computer Systems: Architectures, MOdeling, and Simulation, LNCS XXX, 2006.
- BC21** J. Lee, K. Choi and N. Dutt, "Synthesis of Instructions Sets for High-Performance and Energy-Efficiency," in *Embedded Processor Design - A Low Power Perspective*, Sri Parameswaran and Joerg Henkel, Editors, Springer Academic Pulishers, 2006.

JOURNAL ARTICLES

- J1** D.D. Gajski, N.D. Dutt and B.M. Pangrle, "Silicon Compilation," *Journal of Semicustom ICs*, Vol. 4, No. 2, December 1986, pp. 5-21.
- J2** N.D. Dutt and D.D. Gajski, "Design Synthesis and Silicon Compilation," *IEEE Design and Test of Computers*, December 1990, pp. 8-23.
- J3** N.D. Dutt, "A Language for Designer Controlled Behavioral Synthesis," *INTEGRATION: The VLSI Journal*, No. 16, 1993, pp. 1-31.
- J4** P.K. Jha and N.D. Dutt, "Rapid Estimation for Parameterized Components in High-Level Synthesis," *IEEE Transactions on VLSI Systems*, September 1993, pp. 296-303.
- J5** D.D. Gajski and N.D. Dutt, "Benchmarking and the Art of Synthesis Tool Comparison," *IFIP Transactions A: Computer Science and Technology*, Vol. A-22, 1993 (modified version of paper C10).
- J6** R. Ang and N.D. Dutt, "A Representation for the Binding of RT-Component Functionality to HDL Behavior," *IFIP Transactions A: Computer Science and Technology*, Vol. A-32, 1993 (modified version of paper C15), pp. 263-280.
- J7** N.D. Dutt and P.K. Jha, "Generic RT Component Sets for High-Level Design Applications," *VLSI Design*, Vol. 5, No. 2, 1997, pp. 155-165.
- J8** N.D. Dutt, R. Camposano, D. Agnew, H. Yasuura, A. Domic and M. Wiesel, "Design Reuse: Fact or Fiction?" *IEEE Design and Test of Computers*, Winter 1994 (ACM-SIGDA/D&T Roundtable Summary), pp. 70-77.
- J9** A. Capitanio, N.D. Dutt and A. Nicolau, "Partitioning of Variables for Multiple-Register-File Architectures via Hypergraph Coloring," *IFIP Transactions: Parallel Architectures and Compilation Techniques*, Vol. A-50, 1994, pp. 319-322.
- J10** P.K. Jha and N.D. Dutt, "High-Level Library Mapping for Arithmetic Components," *IEEE Transactions on VLSI Systems*, Vol. 4, No. 2, June 1996, pp. 1-13.
- J11** A. Capitanio, A. Nicolau and N.D. Dutt, "A Hypergraph-Based Model for Port Allocation on Multiple-Register-File VLIW Architectures," *International Journal of Parallel Programming*, Vol. 23, No. 6, 1995, pp. 499-513.
- J12** P.K. Jha, S. Parameswaran and N.D. Dutt, "Reclocking Controllers for Minimum Execution Time," *IEICE Transactions Special Issue on VLSI Design and CAD Algorithms*, Vol. E78-A, No. 12, December 1995, pp. 1715-1722.
- J13** D.J. Kolson, A. Nicolau, N.D. Dutt and K. Kennedy, "Optimal Register Assignment to Loops for Embedded Code Generation," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 1, No. 2, April 1996.
- J14** D.J. Kolson, A. Nicolau and N.D. Dutt, "Elimination of Redundant Memory Traffic in High-Level Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 11, November 1996.
- J15** S.Y. Ohm, F.J. Kurdahi and N. Dutt, "A Unified Lower Bound Estimation Technique for High-Level Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 5, May 1997.
- J16** P.R. Panda, N.D. Dutt and A. Nicolau, "Memory Data Organization for Improved Performance in Embedded Processor Applications," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 2, No. 4, October 1997.

- J17** P.R. Panda, N.D. Dutt and A. Nicolau, "Incorporating DRAM Access Modes into High-Level Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 17, No. 2, pp. 96-109, February 1998.
- J18** P.R. Panda and N.D. Dutt, "Low Power Memory Mapping through Reducing Address Bus Activity," *IEEE Transactions on VLSI Systems*, Vol. 7, No. 3, pp. 309-320, September, 1999.
- J19** P.K. Jha and N.D. Dutt, "High-Level Library Mapping for Memories" *ACM Transactions on Design Automation of Electronic Systems*. Vol. 5, No. 3, pp. 566-603, July 2000.
- J20** P.R. Panda, N.D. Dutt and A. Nicolau, "On-Chip vs. Off-Chip Memory: The Data Partitioning Problem in Embedded Processor-based Systems," *ACM Transactions on Design Automation of Electronic Systems*. Vol. 5, No. 3, pp. 682-704, July 2000.
- J21** P.R. Panda, N.D. Dutt and A. Nicolau, "Local Memory Exploration and Optimization in Embedded Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 1, pp. 3-12, January 1999.
- J22** P.R. Panda, H. Nakamura, N.D. Dutt and A. Nicolau, "Augmenting Loop Tiling with Data Alignment for Improved Cache Performance," *IEEE Transactions on Computers*, Vol. 48, No. 2, pp. 142-149, February 1999.
- J23** A. Khare, P.R. Panda, N.D. Dutt, and A. Nicolau, "High-Level Synthesis with SDRAMs and RAMBUS DRAMs," *IEICE Transactions Fundamentals Special Section on VLSI Design and CAD Algorithms*, Vol. E82-A, No. 11, November 1999, pp. 2347-2355.
- J24** H. Wang, N.D. Dutt and A. Nicolau, "Exploring Scalable Schedules for IIR Filters with Resource Constraints," *IEEE Transactions on Circuits and Systems, Part II*, Vol. 46, No. 11, pp. 1367-1379, November 1999.
- J25** A. Halambi, A. Khare, N. Savoiu, P. Grun, N. Dutt and A. Nicolau, "VSAT: A Visual Specification and Analysis Tool for System-On-Chip Exploration," *Journal of Systems Architecture, Special Issue on Modern Methods and Tools in Digital System Design*, 2000.
- J26** P.R. Panda, N.D. Dutt, A. Nicolau, F. Catthoor, A. Vandecappelle, E. Brockmeyer, C. Kulkarni and E. DeGreef, "Data Memory Organization and Optimizations in Application-Specific Systems," *IEEE Design and Test of Computers*, Vol. 18, No. 3, May-June 2001.
- J26** F. Catthoor, K. Danckaert, S. Wuytack, and N.D. Dutt, "Code Transformations for Data Transfer and Storage Exploration Preprocessing in Multimedia Processors," *IEEE Design and Test of Computers*, Vol. 18, No. 3, May-June 2001.
- J27** P.R. Panda, F. Catthoor, N.D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandecappelle, and P.G. Kjeldsberg, "Data and Memory Optimization Techniques for Embedded Systems," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 6, No. 2, pp. 149-206, April 2001.
- J29** N.D. Dutt, and K. Choi, "Configurable Processors for Embedded Computer," *IEEE Computer*, Vol. 36, No. 1, pp. 120-123, January 2003.
- J30** J. Lee, K. Choi, and N.D. Dutt, "Compilation Approach for Coarse-grain Reconfigurable Architectures," *IEEE Design and Test of Computers, Special Issue on Application Specific Processors*, pp. 26-33, January/February 2003.
- J31** P. Grün, N. Dutt and A. Nicolau, "Access Pattern-Based Memory and Connectivity Architecture Exploration," *ACM Transactions on Embedded Computing Systems (TECS)*, Vol. 2, No. 1, pp. 33-73, February 2003

- J32** P. Grün, A. Halambi, N.D. Dutt, and A. Nicolau, "RTGEN: An Algorithm for Automatic Generation of Reservation Tables from Architectural Descriptions," *IEEE Transactions on VLSI Systems*, pp. 731-737, August 2003.
- J33** M. Mamidipaka, D. Hirschberg and N.D. Dutt, "Adaptive Low Power Encoding Techniques using Self Organizing Lists," in *IEEE Transactions on VLSI Systems*, Special Issue on Low Power Systems, Vol. 11, No. 5, pp. 827-834, October 2003.
- J34** P. Mishra, N.D. Dutt and H. Tomiyama, "Towards Automatic Validation of Dynamic Behavior in Pipelined Processor Specifications," in *Kluwer Design Automation for Embedded Systems (DAES)*, June - September 2003, Volume 8, Issue 2-3, pp. 249-265.
- J35** S. Gupta, N.D. Dutt, R.K. Gupta, A. Nicolau, *Dynamically Increasing the Scope of Code Motions during the High-Level Synthesis of Digital Circuits*, *IEE Proceedings: Computers and Digital Techniques*, (Vol. 150, No.5, Sep 2003 (invited paper).
- J36** S. Pasricha, S. Mohapatra, M. Luthra, N.D. Dutt and N. Venkatasubramanian, "Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices," Special Issue of the Journal of the Korean Multimedia Society (KSSM), Vol. ISSN 12, Dec. 2003, pp. 1-13.
- J37** S. Gupta, N. Savoiu, N.D. Dutt, R.K. Gupta, A. Nicolau, *Using Global Code Motions to Improve the Quality of Results for High-Level Synthesis*, *IEEE Transactions on Computer-Aided Design*, pp. 302-311, Vol 23, No. 2, Feb 2004.
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- C108** M. Reshadi and N.D. Dutt, "Reducing Compilation Time Overhead in Compiled Simulators," *International Conference on Computer Design (ICCD)*, October 2003.
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- C116** S. Gupta, N.D. Dutt, R. Gupta and A. Nicolau, "Loop Shifting and Compaction for the High-Level Synthesis of Designs with Complex Control Flow," *Proceedings of the 2004 Conference on Design, Automation and Test in Europe (DATE 2004)*, February 2004.
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- C118** I. Issenin, E. Brockmeyer, M. Miranda and N.D. Dutt, "Data Reuse Analysis Techniques for Software-Controlled Memory Hierarchies," *Proceedings of the 2004 Conference on Design, Automation and Test in Europe (DATE 2004)*, February 2004.
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- C122** S. Banerjee and N.D. Dutt, "FIFO Power Optimization for On-Chip Networks," *Proceedings of the International Great Lakes VLSI Conference (GLVLSI-2004)*, Boston, April 2004.
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PREMIER REFEREED WORKSHOPS

- W1** N.D. Dutt, "A Language for Designer Controlled Behavioral Synthesis," *1989 ACM/IEEE Physical Design Workshop*, Long Beach, CA, May 2, 1989 (*Invitation-only workshop*).
- W2** N.D. Dutt, "Annotated Textual State Tables: An Intermediate Representation for Synthesis," *IEEE Design Automation Workshop*, Scottsdale, AZ, Jan 22, 1990 (*Invitation-only workshop*).
- W3** N.D. Dutt and J.R. Kipps, "Bridging High Level Synthesis to RTL Technology Libraries," *ACM/IEEE Fifth International Workshop on High Level Synthesis*, Buehlerhoehe, Germany, March 1991 (*Refereed by Program Committee*).
- W4** P.K. Jha and N.D. Dutt, "Rapid Estimation for Parameterized Components in High-Level Synthesis," *ACM/IEEE Sixth International Workshop on High Level Synthesis*, Dana Point, CA, November 1992 (*Refereed by Program Committee*).
- W5** P.K. Jha and N.D. Dutt, "Generic Component Sets and Rapid Technology Projection for High-Level Design Applications," *The 4th ACM/IEEE Physical Design Workshop*, Lake Arrowhead, CA, April 1993 (*Refereed by Program Committee*).
- W6** C. Ramachandran, P.K. Jha, F. Kurdahi and N.D. Dutt, "The Effects of Variations in Component Styles and Shapes on Functional Synthesis," *Proceedings of The International IFIP Workshop on Logic and Architecture Synthesis*, Grenoble, France, December 1993.
- W7** N.D. Dutt, "High-Level Synthesis for Real Architectures -- An Academic HLS View," *1994 IEEE Winter VLSI Workshop*, La Jolla, CA, April 1994 (*Invited talk*).
- W8** S. Novack, A. Nicolau and N.D. Dutt, "A Unified Code Generation Approach Using Mutation Scheduling," *First Workshop on Code Generation for Embedded Processors*, Schloss Dagstuhl, Germany, August 1994 (*Invited talk and paper*).
- W9** D. Kolson, A. Nicolau and N.D. Dutt, "Register Allocation for Embedded Processors with Non-Uniform Register Files," *Second Workshop on Code Generation for Embedded Processors*, Belgium, March 1996 (*Invited talk*).
- W10** N.D. Dutt, "Software Synthesis for Embedded Systems: What's new?," *1996 Dagstuhl workshop on Design Automation for Embedded Systems*, Schloss Dagstuhl, Germany, April 1996.
- W11** N.D. Dutt, Position Statement at the *National Science Foundation Workshop on Future Research Directions in CAD for Electronic Systems*: "Putting the 'D' Back in CAD," Seattle, WA, May 13-14, 1996.
- W12** A. Halambi, A. Nicolau and N.D. Dutt, "Retaining Semantic Information for Improved Code Generation," *Third Workshop on Code Generation for Embedded Processors*, Haus Bommerholz, Witten, Germany, March 1998 (*Invited talk*).
- W13** P. Grün, A. Nicolau & N.D. Dutt, "Automatic Generation of a Software Toolkit from EXPRESSION," *Fourth Workshop on Software and Compilers for Embedded Systems*, St. Goar, Germany, August 1999. (*Invited talk*).

- W14** A. Halambi, N.D. Dutt and A. Nicolau, "Customizing Software Toolkits for Embedded System-On-Chip," *International IFIP Workshop on Distributed and Parallel Embedded Systems(DIPES2000)*, Paderborn University, Germany, October 2000.
- W15** P. Grun, N.D. Dutt and A. Nicolau, "Aggressive Memory-Aware Compilation," *The 2nd Workshop on Intelligent Memory Systems*, In conjunction with *ASPLOS-IX*, Boston Massachusetts, November 12, 2000 (Reviewed by Program Committee)
- W16** A. Halambi, A. Shrivastava, N.D. Dutt and A. Nicolau, "A Customizable Compiler Framework for Embedded Systems," *Fifth Workshop on Software and Compilers for Embedded Systems (SCOPES 2001)*, St. Goar, Germany, March 2001 (Reviewed by Program Committee).
- W17** P. Mishra, F. Rousseau, N.D. Dutt and A. Nicolau, "Architecture Description Language Driven Design Space Exploration in the Presence of Coprocessors," *Proceedings of the 10th (SASIMI 2001)*, October 2001.
- W18** P. Mishra, N. Krishnamurthy, N. Dutt and M. Abadir, "A Property Checking Approach to Microprocessor Verification using Symbolic Simulation," *Microprocessor Test and Verification (MTV)*, Austin, Texas, June 2002.
- W19** R. Cornea, S. Mohapatra, N.D. Dutt, R.K. Gupta, I. Kreuger, A. Nicolau, D. Schmidt, S.K. Shukla, and N. Venkatasubramanian, "A Model-Based Approach to System Specification for Distributed Real-time and Embedded Systems," *9th IEEE Real-time/Embedded Technology and Applications Symposium Workshop on Model-Driven Embedded Systems, (RTAS 2003)*, Washington, D.C., May 2003.
- W20** S. Mohapatra, R. Cornea, N.D. Dutt, A. Nicolau, and N. Venkatasubramanian, "Power-Aware Multimedia Streaming in Heterogenous Multi-User Environments," *IFIP/IEEE International Workshop on Concurrent Information Processing and Computing (CIPC 2003)* Sinaia, Romania, July 2003.
- W21** R. Cornea, N.D. Dutt, R. Gupta, S. Mohapatra, A. Nicolau, C. Pereira, S. Shukla and N. Venkatasubramanian, "ServiceFORGE: A Software Architecture for Power and Quality Aware Services," *International Workshop on Service-Based Software Engineering (co-located with Formal Methods in Europe – FME)*, Pisa, Italy, September 2003.
- W22** S. Pasricha, S. Mohapatra, M. Luthra, N.D. Dutt and N. Venkatasubramanian, "Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices," *First Workshop on Embedded Systems for Real-Time Multimedia*, Newport Beach, CA, October 3-4 2003.
- W23** H. Tomiyama, H. Takada and N.D. Dutt, "Data Organization Exploration for Low Energy Address Buses," *First Workshop on Embedded Systems for Real-Time Multimedia*, Newport Beach, CA, October 3-4 2003.
- W24** N. Bansal, S. Gupta, N.D. Dutt and A. Nicolau, "Analysis of Coarse-Grain Reconfigurable Architectures with Different Processing Element Configurations," *Second Workshop on Application-Specific Processors (WASP'03)*, San Diego, CA, Dec. 2003.
- W25** R. Cornea, S. Mohapatra, N.D. Dutt, A. Nicolau, and N. Venkatasubramanian, "Managing Cross-Layer Constraints for Interactive Mobile Multimedia," *Workshop on Constraint-aware Embedded Software*, Cancun, December 2003.
- W26** Partha Biswas, Sudarshan Banerjee, Nikil Dutt, Laura Pozzi, and Paolo Ienne, "Fast Automated Generation of High-Quality Instruction Set Extensions for Processor Customization," *Third Workshop on Application-Specific Processors (WASP'04)*, Stockholm, Sweden, September 2004. **(BEST PAPER AWARD CANDIDATE)**

- W27** G. Madl and N. Dutt, "Domain-specific Modeling of Power Aware Distributed Real-time Embedded Systems", SAMOS VI: Workshop on Embedded Computer Systems: Architectures, MOdeling, and Simulation, 2006.

PANELS AND TUTORIALS

PANELS

- P1** Panel Statement: "How 'High' is High-Level Synthesis?", *IEEE Computer Society 1992 Workshop on VLSI*, Clearwater Beach, FL, February 2-5, 1992.
- P2** Panel Moderator: "Physical Design Models at the Behavioral Level," *Focused Workshop on Linking Behavioral and Physical Models of Hardware*, Irvine, CA, May 30, 1992.
- P3** Panel Statement: "Hardware/Software Co-Design: Are there any new problems?", *IEEE First Asia Pacific Conference on Hardware Description Languages, Standards and Applications*, Australia, December 1993.
- P4** Panel Organizer & Moderator: "Design Reuse: Fact or Fiction?" *31st ACM/IEEE Design Automation Conference*, San Diego, CA, June 1994.
- P5** Panel Organizer & Moderator: "Impact of Memory Technology and Architectures on System Synthesis," *International Symposium on System Synthesis (ISSS-97)*, Antwerp, Belgium, September 1997.
- P6** Panel Organizer & Moderator: "If Software is King for Systems-on-Silicon, What's New in Compilers?" *ICCD-97: International Conference on Computer Design*, Austin, TX, October 1997.
- P7** Panel Organizer: "IP-Based Design: VIP (Very Important Process) or RIP (Rest in Peace)?" *International Symposium on System Synthesis (ISSS-98)*, Hsinchu, Taiwan, December 1998.
- P8** Panel Organizer: "Driving Agenda in Systems Research," *International Symposium on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2003)*, Newport Beach, CA, Oct. 2003.

TUTORIALS AT CONFERENCES

- TC1** "Design Representation in Synthesis," presented at the *1989 VHDL Users' Group Meeting*, Redondo Beach, CA, October 1989.
- TC2** "High Level Design Synthesis: Specifications, Algorithms and Tools," presented at the *27th ACM/IEEE Design Automation Conference*, June, 1990.
- TC3** "High-Level Chip and System Synthesis," presented at the *IEEE Asia-Pacific Conference on Circuits and Systems 1992 (APCCAS 92)*, December 1992.
- TC4** "High-Level Synthesis," *4th International IFIP 10.5 Working Conference on Electronic Design Automation Frameworks*, Gramado, Brazil, December 1994 (*Invited Tutorial*).
- TC5** "High-Level Synthesis," *4th International Conference on VLSI and CAD (ICVC-95)*, Seoul, Korea, October 1995 (*Invited Tutorial*).
- TC6** "High-Level Synthesis," *IFIP WG 10 State-of-the-Art Seminar Series*, Bangalore, India, January 1996 (*Invited Tutorial*).

- TC7** "ILP Compilation Techniques for Embedded Processors," presented at the *Design, Automation and Test in Europe (DATE'98) Conference*, February 1998.
- TC8** "Embedded Memories in System Design - From Technology to Systems Architecture," presented at the *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-98)*, November 1998.
- TC9** "Embedded Memories in System Design - From Technology to Systems Architecture," presented at the *36th ACM/IEEE Design Automation Conference*, June 1999.
- TC10** "Embedded Memory in Systems - From Architecture to Design Technology," presented at the *Design, Automation, and Test in Europe (DATE'2000) Conference*, March 2000.
- TC11** "System and Architecture-level Power Reduction of Microprocessor-based Communication and Multi-media Applications," embedded tutorial presented at the *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2000)*, November 2000.
- TC12** "Embedded Memories in System Design: Technology, Application, Design and Tools," presented at the *VLSI Design 2001 Conference*, Bangalore, India, January 2001.
- TC13** "New Directions in Compiler Technology for Embedded Systems," presented at the *Asia and South Pacific Design Automation Conference (ASP-DAC 2001)*, Yokohama, Japan, January 2001.
- TC14** "What's New in Compilers for Embedded Systems?" presented at the *XIV Symposium on Integrated Circuits and System Design (SBCCI-2001)*, Brasilia, Brazil, September 2001.
- TC15** "Low-Power/Low Energy Embedded Software: What, Why and How?" presented at the *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2001)*, November 2001.
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- TC16** "On-Chip Communication Architectures: Current Practice, Research and Trends" presented at the *Asia and South Pacific Design Automation Conference (ASP-DAC 2006)*, Yokohama, Japan, January 2006.
- TC17** "Hardware and Software Techniques for Multimedia Systems" presented at the *International Conference on Multimedia & Expo (ICME 2006)*, July 2006.

COURSES TAUGHT

- ICS 280A: SQ90, Graduate course on Algorithms for High Level Synthesis.
- ICS 280B: SQ91, Graduate course on Timing Issues in Specification and Synthesis of Hardware.
- ICS 280C: FQ92, Graduate course on Digital System Testing and Testable Design.
- ICS 290N: FQ90, WQ91, SQ91, FQ91, WQ92, SQ93, Seminar on Design Languages and Representations.
- ICS 299: Every Quarter Since FQ 90, Independent Study.
- ICS 53: SQ00, SQ01, Embedded Computing Systems.
- ICS 151: FQ90, FQ91, SQ93, FQ94, FQ95, WQ97, FQ97, FQ00, SQ02, FQ03, FQ04, WQ05, FQ05 Undergraduate Introductory Course on Logic Design.
- ICS 155A: SQ89, FQ89, SQ93, WQ95, FQ95, FQ96, WQ97 Undergraduate Laboratory Course on Logic Design.
- ICS 180D: SQ92, Introduction to Hardware Description Languages.

ICS 198: SQ89, FQ89, WQ90, SQ90, WQ91, SQ91, FQ91, WQ92, WQ96, FQ96, WQ97, SQ97, FQ97, WQ98, SQ98, SQ99, FQ02, WQ03, SQ03 Undergraduate Honor Program.

ICS 199: FQ89, WQ90, SQ90, WQ91, SQ91, FQ91, WQ92, SQ93, WQ96, FQ96, SQ97, SQ98, WQ99, SQ99, FQ01, WQ02, SQ02 Undergraduate Project Course.

ICS226 (now ICS 253): WQ90, SQ91, SQ92, FQ93, WQ95, FQ96, SQ00 Graduate course on Modeling and Design Description Languages.

ICS227 (now ICS 256): SQ93, FQ95, SQ98, SQ02 Graduate course on Design Synthesis.

ICS 251: SQ01, Graduate course on digital system testing and verification.

ICS 212: SQ05, FQ05 Graduate course on Introduction to Embedded and Ubiquitous Systems.

ICS259: WQ94, FQ94, WQ96, FQ96, SQ97, FQ97, every quarter between FQ98-SQ03, FQ03, SQ04, FQ04: Topics in Design Science.

ICS 202: FQ97, Introductory Seminar for ICS Graduate Students.

ICS 291: FQ97, WQ98, SQ98, FQ99, WQ00, SQ00, FQ02 Directed Research

ICS 399: FQ97, WQ98, SQ98, FQ99, WQ00, SQ00, University Teaching

ECE 299: FQ01, WQ02, SQ02, FQ02, WQ03, SQ03, FQ03, WQ04, SQ04, SQ05 Independent Research

ECE 298: FQ05 EECS Thesis Supervision

UNI STU 3: SQ05, Freshman Seminar

New Courses Developed and Courses Upgraded

ICS 212: SQ05, Graduate course on Introduction to Embedded and Ubiquitous Systems (new course material developed).

ICS 155A: WQ89, Undergraduate Laboratory Course on Logic Design (new course material developed).

ICS 226: FQ89, Graduate course on Modeling and Design Description Languages.

ICS 180D: SQ92, Undergraduate course on Hardware Description Languages.

ICS 280C: FQ92, Graduate course on Digital System Testing and Testable Design.

ICS 155A: WQ94, Undergraduate Laboratory Course on Logic Design (upgraded with Hardware Description Languages and FPGA prototyping tools).

ICS 53: SQ01, Undergraduate course on Embedded Computer Systems (Developed new lab and course lecture material)

UNIVERSITY SERVICE

University-wide Service:

Executive Committee, Industry-University Cooperative Research Program (IUCRP) for Communication and Networking, , 2005-.

Campus-Level Service:

ORU Internal Review Committee: 5-year review of IGB ORU, October 2005

Council on Educational Policy (CEP), 2002-2005.

Policy Subcommittee, CEP, 2003-2005.

UC LEADS Mentorship Program, Summer 2001, Summer 2003.

Action Committee on Courses, 2000-2002.

Faculty Advisory Committee, Test of English Proficiency (TOEP) Program for non-native English speakers, Summer 2000.

Member, UCI Graduate Council: 1996-1997, 1997-1998.

Chair, Subcommittee on Courses, UCI Graduate Council: 1997-1998.

ICS Representative to the Faculty Senate: 1992-1994, 1994-1996.

Committee on Undergraduate Scholarships, Honors and Financial Aid (CUSHFA): 1993-1995, 1995-1996.

UCI Dissertation Fellowship Award Committee: 1996, 1997, 1998.

UCI Committee on Research: Subcommittee for evaluating Multi-Investigator Research Awards: 1998.

ICS Representative to the UCI Defense Conversion Committee: 1993.

Co-Founder, Irvine Research Unit in Computer Systems Design, UCI with N. Bagherzadeh, L. Bic, D. Blough, D. Gajski, K. Kim, F. Kurdahi, A. Nicolau and T. Suda: 1990.

Graduate Minority Mentorship Program: 1993-1994.

Graduate Minority Summer Mentorship Program, Summer: 1991.

Pregraduate Mentorship Program (for minority students): 1990-1991.

School-Level Service:

Chair, SICS Space Committee, 2003-2004, 2004-2005, 2005-2006

Member, SICS Endowed Chair Search Committee: 2003-2004, 2004-2005, 2005-2006

Departmental Service:

Member, CS Undergraduate Committee, 2003-2004

Member, CS PhD Committee, 2003-2004

Vice-Chair, Division of Systems, Department of Computer Science, July 2003-2004

Chair, Ad-Hoc Committee for Promotion Case, 2003-2004, 2004-2005

Member, Ad-Hoc Committee for 2 Promotion Cases, 2003-2004

Faculty Mentor for Assistant Professor Eli Bozorgzadeh, 2003-

Chair, ICS Recruiting Committee for Embedded Systems (2 positions), 2002-2003.

ICS New Degree Programs Committee: 2001-2002

Faculty Mentor for Assistant Professor Tony Givargis, 2001-.

Chair, ICS Personnel Committee, 2000-2001.

Graduate Advisor and Associate Chair for Graduate Studies (ICS): 1997-1998, 1999-2000.

ICS Undergraduate Committee: 1989-1990.

ICS Academic Personnel Committee: 1990-1991, 2001-2002.

ICS Computing Resources Committee: 1991-1992.

ICS Graduate Admissions Committee: 1991-1992, 1992-1993, 1993-1994, 1994-1995, 1998-1999, 1999-2000, 2001-2002.

Chair, ICS Graduate Policy & Admissions: 1995-1996, 1996-1997.

ICS Space Committee: 1992-1993, 1993-1994, 1994-1995.

ICS Undergraduate Honors Selection Committee: 1993.

Faculty Speaker, ICS Career Day for High School Scholars and Their Families: 1996, 1997

UCI American Indian Summer Institute in Computer Science, *Research Careers in Computer Science*, Participant: 1993.