

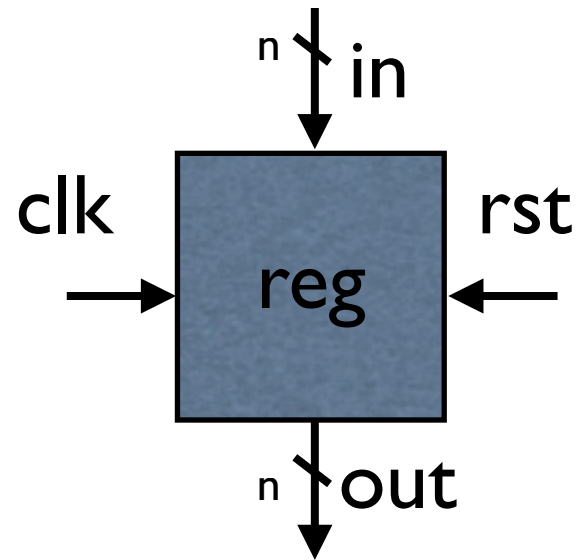
Sequential Circuits

Sequential Circuits

- Circuits that perform a computation in multiple steps (clock cycles)
 - Memory registers
 - Combinational circuits
- Intermediate results are held in registers and transferred from register-to-register using combinational circuits

Memory Register

- Stores n-bits of data
- Rising (or falling) clock latches the input
- Output always maintains the value of stored bit
- May have asynchronous reset



Modeling a Register in VHDL

```
entity REG_8 is
  port(d_i : in UNSIGNED(7 downto 0);
        d_o : out UNSIGNED(7 downto 0);
        clk : in STD_LOGIC;
        rst : in STD_LOGIC);
end REG_8;
```

Modeling a Register in VHDL

```
architecture REG_8_ARCH of REG_8 is
    val : UNSIGNED(7 downto 0);
begin
    process(rst, clk)
    begin
        if( rst = '1' ) then
            val <= "00000000";
        elsif( clk'event and clk = '1' ) then
            val <= d_i;
        end if;
    end process;
    d_o <= val;
end REG_8_ARCH;
```

Modeling an Adder in VHDL

```
entity ADD_8 is
    port(a : in UNSIGNED(7 downto 0);
         b : in UNSIGNED(7 downto 0);
         z : out UNSIGNED(7 downto 0));
end REG_8;
```

Modeling an Adder in VHDL

```
architecture ADD_8_ARCH of ADD_8 is
begin
    process(a, b)
    begin
        z <= a + b;
    end process;
end ADD_8_ARCH;
```

Modeling a Counter in VHDL

```
entity COUNT_8 is
  port (clk : in STD_LOGIC;
        rst : in STD_LOGIC;
        cnt : out UNSIGNED(7 downto 0));
end COUNT_8;
```

Modeling a Counter in VHDL

```
architecture COUNT_8_ARCH of COUNT_8 is
  component REG_8 is
    port(d_i : in UNSIGNED(7 downto 0);
         d_o : out UNSIGNED(7 downto 0);
         clk : in STD_LOGIC;
         rst : in STD_LOGIC);
  end component;
  component ADD_8 is
    port(a : in UNSIGNED(7 downto 0);
         b : in UNSIGNED(7 downto 0);
         z : out UNSIGNED(7 downto 0));
  end component;
  ...
```

Modeling a Counter in VHDL

```
...
    add_a : UNSIGNED(7 downto 0);
    add_b : UNSIGNED(7 downto 0);
    add_z : UNSIGNED(7 downto 0);
begin
    U1: REG_8(add_z, add_a, clk, rst);
    U2: ADD_8(add_a, add_b, add_z);
    add_b <= "00000001";
    cnt <= add_a;
end COUNT_8_ARCH;
```

Complex Sequential Circuits

- Once you go beyond simple devices (e.g., counters), you need a systematic methodology to design sequential circuits
 - Finite state, algorithms, flow charts, etc.
- Processors are sequential circuits
 - Single-purpose
 - General-purpose

Final Notes

- A sequential circuit may have many paths from one register to another
- The delay of the longest path determines the clock speed
- The number of bits of memory in a sequential circuit determines the complexity of the circuit in the number of states