

# Curriculum Vitae

## Elaheh (Eli) Bozorgzadeh

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Computer Science Department  
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### ***Education***

#### **University of California, Los Angeles, CA**

PhD degree in Computer Science: September 2003

#### **Northwestern University, Evanston, IL**

M.S. degree in Electrical and Computer Engineering: December 2000

#### **Sharif University of Technology, IRAN**

B.S. degree in Electrical Engineering: April 1998

### ***Employment***

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#### Assistant Professor

Computer Science Department- Systems division  
University of California, Irvine

Aug. 2003- present

#### Graduate Student Researcher

Computer Science Department, UCLA  
PhD Advisor: Prof. Majid Sarrafzadeh

Jan. 2001-Aug. 2003

#### Summer Intern

Monterey Design Systems, Sunnyvale, CA

Jun. 2000-Sep. 2000

#### Research Assistant

Electrical and Computer Engineering Department, Northwestern University, IL  
Advisor: Professor Majid Sarrafzadeh

Sep. 1998-Dec. 2000

### ***Awards***

- NSF CAREER Award, "CAREER: System Synthesis for Self-adaptive Reconfigurable Embedded Systems", 2009.
- Best paper award, 2006 IEEE International Conference on Field Programmable Logic and Applications (FPL'06)
- Best paper award nominee, ACM/IEEE Design Automation Conference (DAC'05), 2005
- UCI Faculty Career Development Award for 2006-07
- Best Poster Presentation Award, Graduate Student Poster Sessions, Research Review, Computer Science Department, UCLA, 2001.

- Best Poster Award, Graduate Student Poster Session, 2000 ECE Advisory Board Meeting, ECE Department, Northwestern University

## **Professional Membership**

- ACM member and IEEE Member
- IEEE Society of Women Engineers
- ACM Computer Society
- ACM Special Interest Group (SIGDA)
- UCI Center for Embedded and Computing Systems (CECS)
- Member of Calit2 (California Institute of Telecommunication and Information Technology)

## **Professional Activities**

Organizing committee member:

- Program chair for SIGDA PhD Forum in DAC 2009.
- Publication Chair, IEEE ICCD 2009.
- Program Co-chair for SIGDA PhD Forum in DAC 2008.
- Publicity chair for SIGDA PhD Forum in DAC 2007.

Technical program committee:

- Technical Program committee in EMSOFT, 2009.
- Technical Program committee in ACM/IEEE International Symposium in Low Power Electronic Design (ISLPED), 2009
- Technical program committee in SIGDA PhD Forum in DAC, 2007, 2008.
- Technical program committee ACM/IEEE International Conference on Computer-Aided Design (**ICCAD**), 2004, 2006, 2007, 2008. (*Top tier conference in design automation*)
- Technical Program Committee member of IEEE Conference on Field Programmable Logic and Applications (**FPL**), 2005, 2006, 2007, 2008, 2009. (*Top Tier Conference in FPGAs*)
- Technical Program Committee member, IEEE International Conference on VLSI Design, 2009.
- Technical program committee member, IEEE Symposium on Application Specific Processors (SASP), 2008, 2009.
- Technical Program Committee, IEEE Reconfigurable Architecture Workshop (RAW), 2006, 2007, 2008, 2009.
- Technical program committee, IEEE Symposium on Quality of Electronic Design (ISQED), 2005, 2006, 2007, 2008, 2009.
- Technical program committee, IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), 2007.
- Review committee member of IEEE Symposium of Circuits and Systems (ISCAS), 2004, 2005, 2006, 2007, 2008.
- Technical program committee, IEEE Electronic Design Processes (EDP) Workshop, 2006, 2007, 2008.
- Program subcommittee member of IEEE International Midwest Symposium on Circuits and Systems, 2004.

Session chair:

- Session Chair, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2004, 2005, 2006, 2007, 2008.
- Session Chair, IEEE Conference on Field Programmable Logic and Applications (FPL), 2005.
- Session Chair, IEEE International Conference on Computer Design (ICCD), 2008.
- Session chair in IEEE Symposium on Application Specific Processors (SASP), 2008.

- Session Chair, IEEE Reconfigurable Architecture Workshop (RAW), 2006, 2007.
- National Science Foundation (NSF) Panelist.
- Reviewer for more than 10 conferences (such as DAC, DATE, ASPDAC, and FPGA) and 9 journals in the area of embedded systems and design automation such as IEEE Trans. On CAD (TCAD), IEEE Trans. on VLSI (TVLSI), ACM Trans. on Design Automation (TODAES), IEEE Trans. on Computers (TC), and ACM Trans. on Embedded Systems (TECS).

## **Refereed Publications**

### **Book Chapters:**

**BC3-** E. Bozorgzadeh, A. Kaplan, R. Kastner, S. Ogrenci Memik, and M. Sarrafzadeh, "Optimization for Reconfigurable Systems Using Hierarchical Abstraction", J. Cong and J. R. Shinnerl (Editors). *Multilevel Optimization and VLSI CAD*. Kluwer Academic Publishers, Boston, 2002.

**BC2-** X. Yang, E. Bozorgzadeh, M. Sarrafzadeh, and M. Wang, "Modern Standard-cell Placement Techniques". *Layout Optimization in VLSI Design*, Kluwer Academic Publishers, 2002.

**BC1-** E. Bozorgzadeh, R. Kastner, S. Ogrenci Memik, and M. Sarrafzadeh, "Strategically Programmable Systems ", *The Computer Engineering Handbook*, CRC Press, December 2001.

### **Journal papers:**

**J18-** L. Singhal, S. Oh, and E. Bozorgzadeh, "Statistical Power Profile Correlation for Realistic Thermal-aware Floorplanning", under minor revision for publication in *ACM Transactions on Design Automation of Embedded Systems (TODAES)*.

**J17-** S. Banerjee, E. Bozorgzadeh, J. Noguera, and N. Dutt, "Bandwidth Management in Application Mapping for Dynamically Reconfigurable Architectures", under minor revision for publication in *ACM Transactions on Reconfigurable Technology and Systems (TRETTS)*.

**J16-** S. Banerjee, E. Bozorgzadeh, and N. Dutt, "Exploiting application data-parallelism on dynamically reconfigurable architectures: placement and architectural considerations ", to appear in *IEEE Transactions on VLSI (TVLSI)*.

**J15-** S. Oh, T. Kim, J. Cho and E. Bozorgzadeh, "Speculative Loop-Pipelining in Binary Translation for Hardware Acceleration", *IEEE Transactions on CAD (TCAD)*, pp. 409- 422, No. 3, Vol. 27, 2008.

**J14-** L. Singhal and E. Bozorgzadeh, "Multi-layer Floorplanning for Reconfigurable Designs", in *IET Computers & Digital Techniques*, pp. 276-294, No. 1, Vol. 4, 2007.

**J13-** L. Singhal, E. Bozorgzadeh, and D. Eppstein, "Interconnect Criticality Driven Delay Relaxation", in *IEEE Transactions on CAD (TCAD)*, pp.1803-1817, No. 10, Vol. 26, 2007.

**J12-** S. Banerjee, E. Bozorgzadeh, N. Dutt, "Integrating physical constraints in HW-SW partitioning for architectures with partial dynamic reconfiguration", in *IEEE Transactions on VLSI (TVLSI)*, Vol 14 (11), pp 1189-1202, Nov 2006.

- J11-** S. Ghiasi, E. Bozorgzadeh, P. Huang, R. Jafari, and M. Sarrafzadeh, "A Unified Theory of Timing Budget Management", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 25, No. 11, pp. 2364-2375, November 2006.
- J10-** S. Pasricha, N. Dutt, , E. Bozorgzadeh, M. Ben-Romdhane, " FABSYN: Floorplan-Aware Bus Architecture Synthesis", in *IEEE Transactions on VLSI (TVLSI)*, pp. 241-253 ,Vol. 14, No. 3, 2006.
- J9-** G. Wang, S. Sivaswamy, C. Ababei, K. Bazargan, R. Kastner, and E. Bozorgzadeh, "Statistical Analysis and Design of HARP FPGAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, pp. 2088-2102, Vol. 25, No. 10, 2006.
- J8-** S. Ghiasi, K. Nguyen, E. Bozorgzadeh, M. Sarrafzadeh, "Efficient Timing Budget Management for Accuracy Improvement in a Collaborative Object Tracking System", in *Journal of VLSI Signal Processing for Signal Processing and Video Technology*, 42(1), pp. 43-55. 2006.
- J7-** S. Ogrenci Memik, R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "A Scheduling Algorithm for Optimization and Early Planning in High level Synthesis", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 10, No. 1, pp. 33–57, January 2005.
- J6-** E. Bozorgzadeh, S. Ghiasi, A. Takahashi , and M. Sarrafzadeh, "Optimal Integer Delay Budget Assignment on Directed Acyclic Graphs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 23, No. 7, pp. 1184- 1199 , August 2004.
- J5-** E. Bozrgzadeh, S. Ogrenci Memik, X. Yang, and M. Sarrafzadeh, "Routability-driven Packing : Metrics and Algorithms for Cluster-based FPGAs", in *Journal of Circuits, Systems, and Computers (JCSC)*, Vol. 13, No. 1, pp. 77-100, Feb. 2004.
- J4-** E. Bozorgzadeh, R. Kastner, and Majid Sarrafzadeh, "Creating and Exploiting Flexibility in Rectilinear Steiner Trees", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, pp.605-615, Vol. 22, No. 5, May 2003.
- J3-** R. Kastner, Adam Kaplan, S. Ogrenci Memik, E. Bozorgzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", *ACM Transactions on Design Automation of Embedded Systems (TODAES)*, pp. 605-627, Vol.7, No. 4, October 2002.
- J2-** C. Chen, E. Bozorgzadeh, A. Srivastava, and Majid Sarrafzadeh, "Budget Management with Applications", *Algorithmica*, Vol. 34, No. 3, pp. 261-275, July 2002.
- J1-** R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "Pattern Routing: Use and Theory for Increasing Predictability and Avoiding Coupling", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, pp. 777-790, vol. 21, No. 7, July 2002.

## Conferences:

- C35-** S. Golshan, and E. Bozorgzadeh, "SEU-Aware Resource Binding for Modular Redundancy Based Designs on FPGAs", to appear in *ACM/IEEE International Conference on Design, Automation, and Test in Europe (DATE)*, April, 2009.
- C34-** L. Singhal and E. Bozorgzadeh, " Process Variation Aware System-level Task Allocation using

Stochastic Ordering of Delay Distributions", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 570-574, November 2008.

**C33-** L. Singhal, S. Oh, and E. Bozorgzadeh, "Yield Maximization for System-level Task Assignment and Configuration Selection of Configurable Multiprocessors", in *ACM/IEEE IEEE/ACM international Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 249-254, October 2008.

**C32.** A. Gholamipour, E. Bozorgzadeh, and L. Bao, "Seamless Sequence of Software Defined Radio Designs through Hardware Reconfigurability of FPGAs", in *IEEE International Conference on Computer Design (ICCD)*, pp. 260-265, 2008.

**C31-** L. Singhal, S. Oh, and E. Bozorgzadeh, "Statistical Power Profile Correlation for Realistic Thermal Estimation", in *ACM/IEEE Asia-South Pacific Design Automation Conference (ASPDAC)*, pp. 67-70, January 2008.

**C30-** A. Gholamipour, E. Bozorgzadeh and S. Banerjee, "Energy-aware Co-processor Selection for Embedded Processors on FPGAs", in *International Conference on Computer Design (ICCD)*, pp. 158-163, October 2007.

**C29-** L. Singhal and E. Bozorgzadeh, "Novel multi-layer floorplanning for Heterogeneous FPGAs", in *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 613-616, August 2007.

**C28-** S. Golshan and E. Bozorgzadeh, "Single-Event-Upset Awareness in FPGA Routing", in *Proc. of ACM/IEEE Design Automation Conference (DAC)*, p. 330 – 333, June 2007.

**C27-** S. Banerjee, E. Bozorgzadeh, J Noguera, and N. Dutt, "Selective bandwidth and resource management in scheduling for dynamically reconfigurable architectures", in *Proc. of ACM/IEEE Design Automation Conference (DAC)*, pp. 771 – 776, June 2007.

**C26-** L. Singhal and E. Bozorgzadeh, "Heterogeneous Floorplanner for FPGA", in *IEEE Field Programmable Custom Computing Machines (FCCM)*, pp. 311-312, April 2007.

**C25-** S. Banerjee, E. Bozorgzadeh, J. Noguera, N. Dutt, "Minimizing Peak Power For Application Chains on Architectures with Partial Dynamic Reconfiguration", in *International Conference on Field Programmable Technology (FPT)*, pp. 273 – 276, December 2006.

**C24-** L. Singhal and E. Bozorgzadeh, "Multi-layer Floorplanning on a Sequence of Reconfigurable Designs", in *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 605-612, 2006. **(received the best paper award)**

**C23-** S. Dai and E. Bozorgzadeh, "CAD Tool for FPGAs with Embedded Hard Cores for Design Space Exploration of Future Architectures", in *Proceedings of IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 329-330, April 2006.

**C22-** L. Singhal, and E. Bozorgzadeh, "Physically-aware Exploitation of Component Reuse in Partially Reconfigurable Architectures", in *Proceedings of Parallel and Distributed Processing Symposium (IPDPS-*

RAW), Greece, April 2006.

**C21-** S. Banerjee, E. Bozorgzadeh, and N. Dutt, "PARLGRAN: Parallelism Granularity Selection for Scheduling Task Chains on Dynamically Reconfigurable Architectures", in *ACM/IEEE Asia-South Pacific Design Automation Conference (ASPDAC'01)*, pp.491-496 Japan, January 2006.

**C20-** L. Singhal and E. Bozorgzadeh, "Fast Timing Closure through Interconnect Criticality Driven Delay Relaxation", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 791-796, Nov. 2005.

**C19-** S. Banerjee, E. Bozorgzadeh, N. Dutt, "Physically-aware HW-SW Partitioning for reconfigurable architectures with partial dynamic reconfiguration", in *ACM/IEEE Design Automation Conference (DAC)*, pp. 335 – 340, June 2005

**C18-** S. Pasricha, N. Dutt, , E. Bozorgzadeh, M. Ben-Romdhane, "Floorplan-aware Automated Synthesis of Bus-based Communication Architectures", in *ACM/IEEE Design Automation Conference (DAC)*, pp. 565- 570, June 2005. (***nominated for best paper award***)

**C17-** S. Banerjee, E. Bozorgzadeh, and N. Dutt, "Considering runtime reconfiguration overhead in Task Graph Transformations for dynamically reconfigurable architectures", in *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)* , pp. 273- 274, Napa, April 2005

**C16-** S. Sivaswamy, G. Wang, C. Ababei, K. Bazargan, R.Kastner, and E. Bozorgzadeh, "HARP:Hard-wired Routing Pattern FPGAs", in Proceedings of *ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 21 – 29, Feb. 2005.

**C15-** S. Ghiasi, E. Bozorgzadeh, S. Choudhuri, M. Sarrafzadeh, "A Unified Theory for Timing Budget Management", *ACM/IEEE International Conference on Computer-Aided Design*, pp. 653 – 659, Nov. 2004.

**C14-** E. Bozorgzadeh, S. Ghiasi, A. Takahashi, and M. Sarrafzadeh, "Incremental Timing Budget Management in Programmable Systems", *International Conference on Embedded and Reconfigurable Systems and Architecture*, pp. 240-246, July 2004.

**C13-** S. Ghiasi, K. Nguyen, E Bozorgzadeh, and M Sarrafzadeh, "On Computation and Resource Management in Networked Embedded Systems", *International Conference on Parallel and Distributed Computing and Systems*, pp. 445-451, November 2003.

**C12-** E. Bozorgzadeh, S. Ghiasi, A. Takahashi, and M. Sarrafzadeh, "Optimal Integer Delay Budgeting on Directed Acyclic Graphs", *ACM/IEEE Design Automation Conference (DAC'03)* , pp. 920 - 925 ,2003.

**C11-** E. Bozorgzadeh, S. Ogrenci Memik, R. Kastner, and M. Sarrafzadeh, "Pattern Selection: Customized Block Allocation for Domain-Specific Programmable Systems", *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'02)*, pp. 190-196, June 2002.

**C10-** R. Kastner, S. Ogrenci Memik, E. Bozorgzadeh, and M. Sarrafzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", *ACM/IEEE International Conference on Computer-Aided Design (ICCAD'01)*, pp. 127-130, November, 2001.

**C9-** S. Oğrenci Memik, E. Bozorgzadeh, R. Kastner, and M. Sarrafzadeh, "A Super-Scheduler for Embedded Reconfigurable Systems ", *ACM/IEEE International Conference on Computer-Aided Design (ICCAD'01)*, pp. 391-394, November, 2001.

**C8-** E. Bozorgzadeh, R. Kastner, and M. Sarrafzadeh, "Creating and Exploiting Flexibility in Steiner Trees", *ACM/IEEE 38th Design Automation Conference (DAC'01)*, pp. 195 – 198, June 2001.

**C7-** S. Oğrenci Memik, E. Bozorgzadeh, R. Kastner, and M. Sarrafzadeh, "SPS: A Strategically Programmable System", *Reconfigurable Architecture Workshop (RAW'01)*, April 2001.

**C6-** R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "An Exact Algorithm for Coupling-Free Routing", *ACM/IEEE International Symposium on Physical Design (ISPD'01)*, pp. 10 – 15, April 2001.

**C5-** M. Sarrafzadeh, E. Bozorgzadeh, R. Kastner and A. Srivastava, "Design and Analysis of Physical Design Algorithms ", *ACM/IEEE International Symposium on Physical Design (ISPD'01)*, pp. 82 – 89, April 2001.

**C4-** X. Yang, E. Bozorgzadeh, and M. Sarrafzadeh, "Wirelength and Rent exponents of Partitioning and Placement", *ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP'01)*, pp. 25 – 31, April 2001.

**C3-** E. Bozorgzadeh, S. Oğrenci Memik, and M. Sarrafzadeh, "RPack: Routability-Driven Packing for Cluster-Based FPGAs", *Asia-South Pacific Design Automation Conference (ASPDAC'01)*, pp. 629 - 634, January 2001.

**C2-** R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "Predictable Routing", *ACM/IEEE International Conference on Computer-Aided Design (ICCAD'00)*, pp. 110 – 114, November, 2000.

**C1-** R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "Coupling Aware Routing", *IEEE International ASIC/SOC Conference*, pp. 392-396, September 2000.

### **Poster Presentations (Only Abstracts appeared in the Proceedings)**

**P3-** Soheil Ghiasi, Karlene Nguyen, Elaheh Bozorgzadeh, Majid Sarrafzadeh, "On Computation and Resource Management in an FPGA-based Computing Environment", accepted as poster presentation at *ACM International Symposium on Field-Programmable Gate Arrays (FPGA'03)*, February 2003.

**P2-** E. Bozorgzadeh and M. Sarrafzadeh, "Customized Regular Channel Design in FPGAs", accepted as poster presentation at *ACM International Symposium on Field-Programmable Gate Arrays (FPGA'03)*, February 2003.

**P1-** E. Bozorgzadeh, S. Oğrenci Memik, R. Kastner, and M. Sarrafzadeh, "Pattern Selection in Programmable Systems", poster presentation at *ACM International Symposium of Field Programmable Gate Arrays (FPGA'02)*, Feb. 2002.

### **Grants and Research Support**

**NSF CAREER # 0846129:** System Synthesis for Self-adaptive Reconfigurable Embedded Systems, PI, \$400K, 2009-2013.

**NSF Grant #0725914:** Adaptive Network Assimilations through System Reconfigurability, Co-PI, \$300K. (PI: Luke Bao) (equal contribution) (2007-2010)

University of California MICRO program (industrial sponsor: Conexant Systems Inc.) (2006-2007)  
Proposal Title: Physically-aware Timing Budget Management  
Total Awarded Amount: \$28,750

University of California MICRO program (industrial sponsor: Conexant Systems Inc.) (2005-2006)  
Proposal Title: Design Planning by Timing Budget Management  
Total Awarded Amount: \$25,700

Industry gift:

Conexant Systems Inc. , 2004, Total Amount: \$12,000.00  
Xilinx Software tools and Hardware development boards, 2003-2008,  
[Total Amount ~\$100,000.00]

Departmental Funds:

UCI CORCLR Grant, 2006, Total awarded amount: \$6000.00  
UCI CORCLR Travel Grant (2007), Total Awarded Amount: \$1700.00  
UCI CORCLR Travel Grant (2008), awarded amount: \$2500.00  
UCI Faculty Career Development Award, \$1000.00, 2006-2007.

## ***Teaching and Advising Experience***

### **Courses:**

CS 153 Logic Design Laboratory	Winter'09
ICS-151 Introduction to Digital Design, Computer Science Department, University of California, Irvine.	Spring '04, Spring'05, Spring'06, Winter'07, Fall'07, Winter 2008
ICS-252: Introduction to computer design, Computer Science Department, University of California, Irvine.	Winter'04, Winter'05, Fall'05, Fall'06, Fall'07
ICS 258- Combinatorial Algorithms for Design Synthesis	Fall'04, Spring'06

### **Advising:**

Graduate students:

- Shahin Golshan (PhD candidate) (Expected graduation: Winter 2010)
- Hessam Koori (PhD student) (Expected graduation: Winter 2012)
- Love Singhal (PhD) (graduated in January 2009)
  - Thesis: System Level Design Planning for Parametric Yield Improvement
  - Current Employment: Synopsys
- Sudarshan Banerjee (PhD 2007, co-advised with Prof. Nik Dutt)
  - Thesis: Application Mapping for Platform FPGAs with Partial

### Dynamic Reconfiguration

- (currently at Liga Systems Inc., CA.)
- AmirHossein Gholamipour (advisee during 2005-2007) (currently PhD student at UCI)
- Simin Dai (MS degree, December 2006)  
Thesis: H-FPGA: Heterogeneous FPGA Place and Route  
Current position: Software engineer, Analog Devices Inc., Texas.

### Undergraduate students:

- Richa Prasad (Univ. of Massachusetts, Amherst), Summer'05.
- Jin Wu (Northwestern University), Summer'05.
- Laura Beck (Cornell University), Summer'04.
- Padmini Nagaraj (UC-Berkeley), Summer'04.

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### ***Invited Talks (other than paper presentation in conferences)***

IEEE Computer Society, Orange County Chapter Title: <b>Resource Management in Reconfigurable System-on-Chip Devices</b>	April 23, 2007
Ghent University, Belgium Title: <b>Physical Planning and Resource Management in Reconfigurable SoCs</b>	May 7, 2007
University of Karlsruhe, Germany Title: <b>Physical Planning and Resource Management in Reconfigurable SoCs</b>	May 9, 2007
Conexant Systems Co., Newport Beach, CA Title: <b>Rapid Design Closure in Embedded System Design</b>	March 4, 2004
Xilinx Inc., Mountain View, CA Title: <b>Toward Efficient and Practical Exploitation of Dynamic Reconfigurability in FPGAs</b>	July 22, 2005
Tokyo Institute of Technology, Tokyo, Japan Title: <b>Criticality Driven Timing Budget Management</b>	Jan 30, 2006

### ***UCI Community Service***

- Computer Science and Engineering steering committee, 2006-07, 2007-08.
- Campus-wide UCI Honors program (member), 2007-08.
- ICS undergraduate policy committee, 2006-07.
- SOAR: ICS Student Outreach, Access, and Retention (member), 2005-06.
- ICS Graduate policy (member), 2004-05.
- Curriculum Revision of Computer Science B.S. Degree (member), 2003-04.
- ICS Website design (member), 2003-04.
- Committee member in 31 PhD candidacy exams (chair in three exams)
- Committee member in 6 Topic Defense (chair in one Topic defense)
- Committee member in 4 Final PhD Defense.

### ***Outreach Program Activities***

- CRA-Woman Summer undergraduate research mentorship program, Summer'04, Summer'05
- Sally Ride Science Festivals-- workshop for girls (5<sup>th</sup>-8<sup>th</sup> graders), 2004, 2005, 2006.
- Science and Technology Awareness day, Los Angeles, CA, May 2008.
- Reviewer for Travel Grant for female students attending Grace Hopper Conference, 2007, 2008.
- SIGDA-W sub-committee member, 2009.