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Objective

Obtain a position in a development and/or research firm, and involve in designing latest SoCs for novel applications

Field(s) of interest

Computational neuroscience, computer vision and robotics, reconfigurable and multiprocessor architectures, parallel programming on high-performance architectures, CAD for System-on-Chip (synthesis and verification), embedded system & software design

Academic background

1. **University of California, Irvine,** 2005 - present
PhD Student in Computer Science with Center for Embedded Computing Systems (GPA: 3.9/4)
2. **Indian Institute of Technology, Delhi, India,** 2000 - 2002
Master of Technology in VLSI Design Tools and Technology (CGPA: 9.20/10.0)
3. **Government College of Tech., Coimbatore India,** 1995 - 1999
Bachelor in Electronics and Communication Engineering, (Grade: 89/100)

Work experience

- Graduate Research Assistant, Department of Computer Science, University of California** Jan 06 - present
- Brain inspired computing – Algorithms and Hardware/Software realization
- Summer Intern, Broadcom Corporation, San Diego** July 07 – Sep 07
- Design and Simulation of ARM-Cortex based SoC for Bluetooth systems
- Summer Intern, Freescale Semiconductors, Austin** July 06 – Aug 06
- Dynamic simulation techniques for PowerPC based architecture description languages
- Research Engineer, at Philips Labs, The Netherlands** 2002 - 2005
- Multiprocessor SoC design and verification for Media processing applications
 - HW-SW and Mixed-HW Co-simulation framework for multiprocessor simulation
 - Implementation and optimization of H.264 decoder on Tri-Media VLIW processor
 - Application level performance metrics and implementation for multiprocessors applications
 - Kahn process networks based application modeling for multiprocessors (Graduate/Master thesis)

Selected publications

1. "Efficient Simulation of Large-Scale Spiking Neural Networks using Graphics Processors", *IJCNN, 2009 (Best paper)*
2. "Computing Spike Based Convolutions on GPUs", *Intl. Symposium on Circuits And Systems (ISCAS), 2009*
3. "Scalable Parallel Implementations of a Brain Derived Vision Algorithm", *IJPP issue on Bio/Nano Applications, 2009*
4. "Accelerating Brain Circuit Simulations for Object Recognition with CELL Processor", *IEEE Workshop on Innovative Architectures, 2007,*
5. "Novel Brain-Derived Algorithms Scale Linearly with Number of Processing Elements", *ParaFPGA, 2007,*
6. "A complexity effective communication model for behavioral modeling of signal processing applications", *DAC 2003*
7. "Cache-Coherent Heterogeneous Multiprocessing as basis for Streaming Applications", In: *Dynamic and robust streaming in and between connected CE-devices*", *Book chapter in Kluwers*

Achievements and recognitions

- 1) Best paper award from International Joint Conference in Neural Network, 2009
- 2) IBM CELL/B.E University Challenge 2007 Grand Prize winner
- 3) Two joint patents in multiprocessor architectures and SoC Verification
- 4) All India Rank 3 in Graduate Aptitude Test in Engineering for ECE students among over 10000 candidates (GATE 2001)
- 5) Graduate Fellowship from Philips Semiconductors, The Netherlands for Graduate Master studies in VLSI Design (2001).
- 6) First rank medal for undergraduate students in Department of ECE at Government. College of Tech, INDIA(1999)

Software skills

- Programming: C, C++, Matlab, Verilog, VHDL, SystemC, parallel programming (MPI/Pthreads), scripting languages (perl,python,awk etc), parallel programming on IBM CELL processor, NVIDIA GPUs
- Embedded processor programming: TriMedia, MIPS, 8085/86
- EDATools: Xilinx/Altera FPGA Tools, Synopsys DC tools, Cadence Incisive tools, Magic & Tanner Layout Tools.