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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- Nikil Dutt authors on-chip communication architectures book
- CECS hosts DAC open house
- Project Profile: "Bridging the Gap between Neuron and Silicon"
- Jelena receives Graduate Dean's Dissertation Fellowship

Inside this Issue:

Nikil Dutt and Sudeep Pasricha Author On-Chip Communication Architectures Book

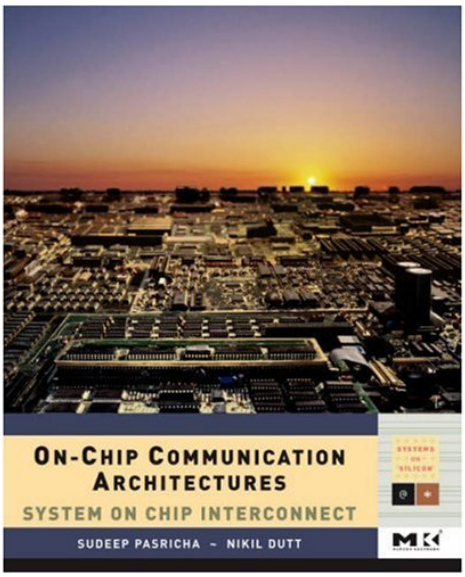
Chancellor's Professor Nikil Dutt and doctoral student Sudeep Pasricha have co-authored the book **On-Chip Communication Architectures: System on Chip Interconnect**. Their book, officially published on April 18, 2008, includes the following topics:

· Definitive guide to on-chip communication architectures for emerging chip multiprocessor systems

· Detailed analysis of all popular standards for on-chip communication

· Comprehensive survey of research on communication architectures, covering a wide range of topics, spanning the past several years and up to date with the most current research

· Overview of future trends that will have a significant impact on communication architecture research and design over the next several years: networks-on-chip, optics, wireless, 3D, carbon nanotube on-chip interconnects



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CECS Hosts DAC Open House

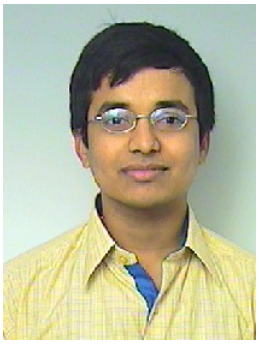
The 45th Design Automation Conference (DAC) was held in Anaheim, CA on June 8-13, 2008. CECS hosted an open house for DAC attendees on Friday afternoon, June 13, 2008 from 2:00PM to 4:00PM in our CECS office on the 2nd floor of the Anteater Instruction & Research Building (AIRB). We had a buffet of sandwiches, cookies, and soft drinks in a relaxed atmosphere. Many of our research affiliates and graduate students were available to informally discuss new directions in technology and research.

DAC attendees were able to see first hand our research programs and visit with our professors and graduate students.

PROJECT PROFILE

Bridging the Gap Between Neuron and Silicon

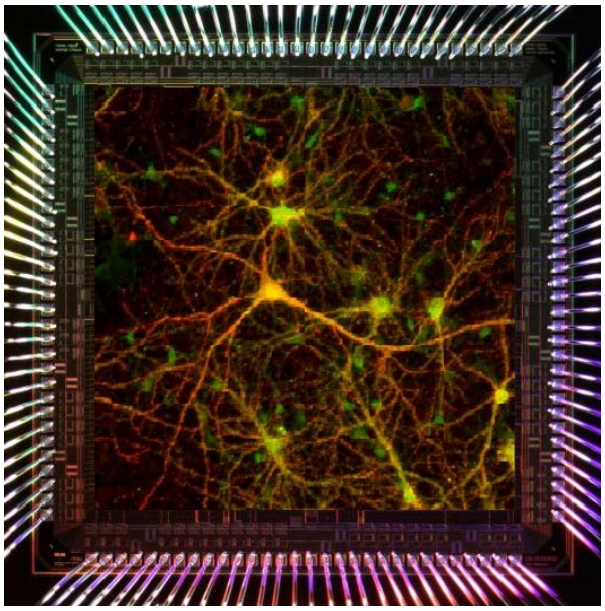
- Jayram Moorkanikara Nageswaran



How do we build the next generation of computing systems? The answer to this question can solve many challenges associated with building smart and efficient computing systems for futuristic applications in vision, robotics, ambient intelligence etc. One area of engineering called "neuromorphic engineering" explores these challenges by building systems inspired by the biological architecture of the brain. Understanding the brain or "reverse engineering the brain" is essential for developing the principles of neuromorphic systems. Interestingly, the National Academy of Engineers (NAE) has also declared that reverse-engineering the brain is one of the grand challenges of the 21st century. We cannot understate the advantages of looking at the ultimate machine ("brain") for building new kinds of systems. First of all we already know that the human brain is about a million times more energy efficient than a supercomputer of equivalent performance. Secondly, even if we did have an equivalent supercomputer it may still not match the brain's capability; for instance in the execution of the vision tasks that can be so effortlessly done by a rat or a house fly. If you look beyond the computational principles that typically interest computer engineers, there are many advantages for better understanding the brain in the area of medicine, artificial intelligence, human-computer interaction and much more (See [1]).

In the BRICS (brain inspired computing systems) project at CECS we are working on understanding and building brain derived systems. A project of this magnitude involves active interdisciplinary collaboration between CECS and computational neuroscientists from various groups. Currently this project is a joint collaboration between the groups of Prof. Nikil Dutt in CECS and Prof. Jeff Krichmar in the UCI Cognitive Science Department. The BRICS project aims to understand new computational principles inspired by brain circuitry, and develop computational platforms for simulation of brain circuitry, as well as programming models for algorithms derived from the principles of brain circuitry.

There are two approaches to understanding and simulating brain circuits: bottom-up and top-down. In the bottom-up approach we start by implementing and simulating the basic elements of brain circuits, namely individual neurons and the properties of the synapses (the point of connection between neurons). The neurons in the brain are of various types but broadly they can be categorized into inhibitory or excitatory neurons. These neurons communicate by means of spikes (or pulses). One can understand and analyze properties of the brain circuit elements by modeling them using the properties of transistors and their interconnection networks in the field of semiconductor physics. Using these basic brain circuit elements, we can build basic canonical circuits. Many types of canonical circuits have been identified in brain circuits. One example is winner-take-all mechanism. In this mechanism, if many neurons are firing simultaneously only a small group of some neurons that are firing very highly is passed on to the next stage. Using similar canonical circuits we can build large scale networks that learn and adapt based on the given task (See [6] for an example). In the top-down approach, the application takes precedence over basic elements. Here a high-level algorithm is derived based on a cortex-like mechanism for the given task (e.g., vision, navigation, audition, etc). Many high-level models of brain circuits have been proposed, including those based on Bayesian networks and feed-forward networks. The advantage of the top-down approach is that it can be easily constructed and applied to many real-world applications.



From a computational perspective, brain inspired algorithms are extremely parallel in nature when compared against conventional algorithms. Hence these brain-inspired algorithms offer both an opportunity, as well as a challenge for effective mapping onto, and simulation using modern multiprocessing platforms. Our research efforts have investigated the use of several multiprocessing platforms for simulation, including conventional computing clusters, modern high-performance architectures such as the IBM CELL, general purpose graphics engines such as the Nvidia CUDA platform, and also reconfigurable fabrics using FPGAs.

The concept of exploiting brain-based algorithms using silicon is not new but has been actively pursued by various researchers,

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FELLOWSHIP AWARD

Jelena Trajkovic receives Graduate Dean's Dissertation Fellowship

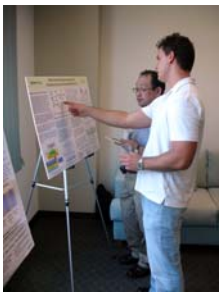
This year the Graduate Dean is awarding a new fellowship for students nearing completion of their dissertations. The recipients are given a monetary award to be used for stipend and fees. The Graduate Dean's office received 35 applications and awarded 13 of these one-quarter fellowships for academic year 2008/2009. One of these recipients is ICS PhD candidate and CECS graduate student researcher Jelena Trajkovic.

Jelena has been co-advised by Prof. Gajski and Prof. Veidenbaum. Her research focus is in the design of embedded systems. She currently works with Prof. Gajski on automating processor core design. She has developed novel techniques for mapping C code to hardware structures. These techniques significantly simplify embedded design process; decrease design time and lead to productivity gains. Under supervision of Prof. Veidenbaum, she developed an architectural technique for reducing energy consumption of main memory in embedded systems, which both increases battery life and speeds up the application execution. She hopes to pursue an academic career where she would educate future generations of computer scientists and electrical engineers.

An article regarding Jelena's fellowship is to appear on http://www.rgs.uci.edu/ later this quarter.

More CECS DAC Open House Pictures

(cont'd from pg. 1)



Embedded Software Blog Launches on CECS web site

The Embedded Software Blog has officially launched on CECS. You will find articles posted by our faculty, students, and staff regarding all things embedded. The blog can be reached by clicking on the link at the very top left navigation bar or via the link below.

If you are a CECS member who wishes to contribute to the blog or have any questions, please contact our webmaster or consult faculty members who are currently contributing, i.e. Professor Tony Givargis, Professor Pai Chou, and others.

All students, faculty, and staff are highly encouraged to participate in the CECS blog. This blog gives everyone the ability to better connect and share ideas with colleagues, opening opportunities for further discussion.

You can reach the blog by visiting http://www.cecs.uci.edu/ or directly at http://www.cecs.uci.edu/esw/.

VISITOR PROFILE

Project Profile (cont'd from page 2)

including Carver Mead at CalTech. In actively trying to bridge the gap between science and engineering, he said "*To understand reality, you have to understand how things work. If you do that, you can start to do engineering with it, build things. And if you can't, whatever you're doing probably isn't good science. To me, engineering and science aren't separate endeavors".*

With tremendous improvements in brain imaging technology, and other neuroscience related discoveries, the idea of realizing computational architectures inspired from the brain is gaining a lot of momentum and interest.

References:

(1) http://www.engineeringchallenges.org/
(2) "The singularity is near" by Ray Kurzweil, Viking Penguin 1999
(3) "Learn like a Human", Jeff Hawkins, IEEE Spectrum, April 2007
(4) "The Computers and the Brain", John Von Neumann
(5) "Accelerating Brain Circuit Simulations of Object Recognition with CELL Processors", A. Felch, J. Moorkanikara, et al., IWIA 2007
(6) "Brain-based Devices Project", vesicle.nsi.edu/nomad

Nikil Dutt and Sudeep Pasricha Author On-Chip Communication Architectures Book (cont'd from front page)

Dutt's research lies at the intersection of compilers, architectures and computer-aided design, with a specific focus on the exploration, evaluation and design of domain-specific embedded systems that span research issues in hardware, software, networked, and ubiquitous systems.

Other projects include low-power/low-energy compilation and synthesis, validation and verification of pipelined processors, software/hardware interfaces for distributed embedded systems, and memory architecture exploration for embedded systems.

Additional information about Professor Dutt and his work can be found on his web site:
http://www.ics.uci.edu/~dutt/

Additional information about Sudeep Pasricha and his work can be found on his web site:
http://www.engr.colostate.edu/~sudeep/

Visitor Profile

JeongKi Kim

Jeongki Kim is visiting CECS for one year, starting July 2008. He is from the Electronics and Telecommunications Research Institute (ETRI, www.etri.re.kr) in Korea. ETRI, sponsored by the Korean government is the largest research institute in South Korea and is researching on several fields of electronics, telecommunications, semiconductor, computer systems, and so forth. At ETRI, he has been working in Embedded Software Division and developing a sensor node OS and a sensor network simulator. The sensor node OS called NanoQplus is a lightweight operating system integrated with several hardware platforms for ubiquitous sensor networks. It is being made to support the effective development of USN applications. Detailed information is referred to the website http://www.qplus.or.kr.

Since his graduation with a Ph.D. degree from Chonbuk National University, Korea in 1999, he has been mainly studying and developing computer software in ETRI. His area of specialization has been concentrated on file systems based on flash memories and hard disks in embedded OS. His team's embedded OS called Qplus is classified into several versions, regular Qplus, NanoQplus, and ESTO. The regular Qplus is an embedded OS to apply to relatively large embedded systems, such as PDA and set-top boxes. ESTO is a development tool for embedded software.

At CECS, he'll join Prof. Chou's lab as a visiting scholar. He'll survey Chou's studies about the structure and mechanism of embedded sensing systems and verify whether the NanoQplus made by ETRI can be applied to them. Also, he'll examine whether his studies at CECS can be utilized in current projects in ETRI or in the next project as a core technique. He said "I'm very happy to work with Prof. Chou, and I want to get a good result from my studies at CECS. I hope to be able to have an opportunity for collaboration with Prof. Chou or CECS with further ETRI projects".

Jeongki said, "This is my first time to stay at USA such a long time although I have an experience visiting Redhat in 2001. I'm excited to visit Irvine that is beautiful, safe, and cultural city. My family is admiring beautiful coasts and wide parks. I'm sure I'll have many chances to experience interesting things and enjoy American cultures."

PUBLICATIONS

The following papers were published by CECS affiliates between April 2008 to August 2008.

Focus	Title, Author, Publication
Execution Locality	Miquel Pericas, Adrian Cristal, Francisco J. Cazorla, Ruden Gonzalez, Alex Veidenbaum, Daniel A. Jimenez, and Mateo Valero, "A Two-Level Load/Store Queue based on Execution Locality," Proc. 35th International Symposium on Computer Architecture (ISCA) June 2008.
Energy Consumption	Carmen Badea, Alexandru Nicolau, and Alexander V. Veidenbaum, "Impact of JVM superoperators on energy consumption in resource-constrained embedded systems," Proc. of the ACM SIGPLAN-SIGBED conference on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2008.
Energy-delay Efficiency	Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, and Alexander V. Veidenbaum, "Dynamic register file resizing and frequency scaling to improve embedded processor performance and energy-delay efficiency," Proc. of the Design Automation Conference (DAC) 2008.
Cache-awareness	Arun Kejariwal, Alexandru Nicolau, Utpal Banerjee, Alexander V. Veidenbaum, Constantine D. Polychronopoulos, "Cache-aware iteration space partitioning," Proc. of the ACM SIGPLAN Symposium on Principles and practice of parallel programming (PPOPP) 2008.
Reducing Energy-delay	Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum, "Improving performance and reducing energy-delay with adaptive resource resizing for out-of-order embedded processors," ACM SIGPLAN/SIGBED 2008 Conference on Languages, Compilers, and Tools for Embedded Systems, LCTES 2008.
Distributed Real-Time Systems	Chongjing Chen and Pai H. Chou, "EcoDAQ: A Case Study of a Densely Distributed Real-Time System for High Data Rate Wireless Data Acquisition," to appear, in Proc. 14th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), 2008. Kaohsiung, Taiwan.
Efficient Supercapacitors	Farhan Simjee and Pai H. Chou, "Efficient Charging of Supercapacitors for Extended Lifetime of Wireless Sensor Nodes," in IEEE Transactions on Power Electronics, Volume 23, Issue 3, May 2008. pages 1526--1536.
System-on-Chip Environment	R. Doemer, A. Gerstlauer, J. Peng, D. Shin, L. Cai, H. Yu, S. Abdi, D. Gajski: "System-on-Chip Environment: A SpecC-Based Framework for Heterogeneous MPSoC Design", EURASIP Journal on Embedded Systems, vol. 2008, article ID 647953, 13 pages, July 2008.
Parallel and Flexible MPSoC	P. Chandraiah, R. Doemer: "Code and Data Structure Partitioning for Parallel and Flexible MPSoC Specification Using Designer-Controlled Recoding", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 6, pp. 1078-1090, June 2008.
Instrumented Cyber Physical Spaces	Minyoung Kim, Daniel Massaguer, Nikil Dutt, Sharad Mehrotra, Shangping Ren, Mark-Oliver Stehr, Carolyn Talcott, Nalini Venkatasubramanian, "A Semantic Framework for Reconfiguration of Instrumented Cyber Physical Spaces", Second Workshop on Event-based Semantics (WEBS'08) in conjunction with IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'08) in part of CPSWEEK, Apr. 2008, St. Louis, MO, USA
Code-Modulated Path-Sharing	Fred Tzeng, Amin Jahanian, Deyi Pi, Payam Heydari, "A CMOS Code-Modulated Path-Sharing Multi-Antenna Receiver Front-End for Spatial Multiplexing, Spatial Diversity and Beamforming," IEEE RFIC Symposium, June 2008. (Nominated for the Best Paper Award).
Code-Modulated Path-Sharing	Fred Tzeng, Amin Jahanian, Payam Heydari, "A Universal Code-Modulated Path-Sharing Multi-Antenna Receiver Architecture," IEEE Wireless Communications & Networking Conference (WCNC), April 2008.
ESL Hand-off	N. Dutt, "ESL Hand-off: Fact or EDA Fiction?" Panel Position Statement, Proceedings of the Design Automation Conference 2008 (DAC 2008), Anaheim, CA, June 2008.

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PUBLICATIONS (cont'd from pg 5)

The following papers were published by CECS affiliates during Winter 2008 quarter

Focus	Title, Author, Publication
Energy Efficiency	J. Trajkovic, A. Veidenbaum, A. Kejariwal 'Improving SDRAM Access Energy Efficiency for Low-Power Embedded Systems,' In ACM Transactions on Embedded Computing Systems (Apr. 2008).
Processor Core Construction	J. Trajkovic, D. Gajski 'Custom Processor Core Construction from C Code,' In Proceedings of Sixth IEEE Symposium on Application Specific Processors (June 2008)
Speculative Execution	Dongsoo Kang, Chen Liu, and Jean-Luc Gaudiot, "The Impact of Speculative Execution on SMT Processors," International Journal of Parallel Programming (IJPP), Volume 36, Number 4, August 2008.
Speculative Pre-Execution	Won Woo Ro and Jean-Luc Gaudiot, "A Low-Complexity Microprocessor Design with Speculative Pre-Execution," Journal of System Architecture July 07, 2008.
Simultaneous MultiThreading Microarchitectures	Chen Liu and Jean-Luc Gaudiot, "Resource Sharing Control in Simultaneous MultiThreading Microarchitectures," Proceedings of the 13th Asia-Pacific Computer Systems Architecture Conference (ACSAC '08), Hsinchu, Taiwan, August 04 - 06, 2008.
Modern Parallel Machines	Shaoshan Liu and Jean-Luc Gaudiot , "The Potential of Fine-Grained Value Prediction in Enhancing the Performance of Modern Parallel Machines ," Proceedings of the 13th Asia-Pacific Computer Systems Architecture Conference (ACSAC '08), (Best Paper Award), Hsinchu, Taiwan, August 04 - 06, 2008.
Prefetch-Based DSM Systems	Hsiao-Hsi Wang, Kuan-Ching Li, Ssu-Hsuan Lu, Chun-Chieh Yang, Jean-Luc Gaudiot , "Design and Implementation of an Agent Home Scheme Strategy for Prefetch-Based DSM Systems," International Journal of Parallel Programming (IJPP), Springer.
On-Chip Communication	S. Pasricha, N.D. Dutt, "On-chip Communication Architectures: Current Practice, Research and Future Trends," Morgan Kaufman/Elsevier Systems-on-Silicon Series, 2008.
Processor Description	P. Mishra, N.D. Dutt, "Processor Description Languages: Applications and Methodologies," Morgan Kaufman/Elsevier Systems-on-Silicon Series, 2008.
Pipelined Processors	P. Mishra and N.D. Dutt, "Specification-driven Directed Test Generation for Validation of Pipelined Processors," ACM Transactions on Design Automation of Electronic Systems (ACM-TODAES), Vol. 13, No. 2, Article 42 (July 2008), 36 pages, DOI = 10.1145/1367045.1367051.
Communication Architecture	I. Issenin, E. Brockmeyer, B. Durninck and N. Dutt, "Data Reuse Driven Energy-Aware Co-Synthesis of Scratch Pad Memory and Hierarchical Bus Based Communication Architecture for Multiprocessor Streaming Applications" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 27, No. 8, August 2008, pp. 1439-1452.
Array Access Patterns	D. Cho, I. Issenin, S. Pasricha, N. Dutt, and Y. Paek, "Compiler Driven Data Layout Optimization for Regular/Irregular Array Access Patterns," Proceedings of ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES08) , June 2008.
System Level Performance Analysis	S. Pasricha, N. Dutt, and F. Kurdahi. "System Level Performance Analysis of Carbon Nanotube Global Interconnects for Emerging Chip Multiprocessors," Proceedings of the IEEE/ACM International Symposium on NanoScale Architectures (NanoArch 2008), Anaheim, CA, June 2008.
Photon Migration Instrument	Keun-Sik No, Richard Kwong, Pai H. Chou, and Albert Cerussi, "Design and Test of a Miniature Broadband Frequency Domain Photon Migration Instrument," to appear, Journal of Biomedical Optics, SPIE, Accepted for publication.
RTL Synthesis	D. Shin, A. Gerstlauer, R. Doemer, D. Gajski: "An Interactive Design Environment for C-based High-level Synthesis of RTL Processors", IEEE Transactions on Very Large Scale Integration Systems, vol. 16, no. 4, pp. 466-475, April 2008.

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***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Publications (cont'd from page 6)

Focus	Title, Author, Publication
System Level Modeling	Weiwei Chen, Siwen Sun, Bin Zhang, Rainer Doemer, "System Level Modeling of a H.264 Decoder," TR 08-10, August 12, 2008.
Mobile Multimedia Systems	Kyoungwoo Lee, Aviral Shrivastava, Minyoung Kim, Nikil Dutt, Nalini Venkatasubramanian, "Cross-Layer Interactions of Error Control Schemes in Mobile Multimedia Systems," TR 08-09, July 28, 2008.
Kahn Process Networks	Ines Viskic and Daniel Gajski, "Modeling Kahn Process Networks on MPSoC Platforms," TR 08-08, July 11th, 2008.
Multiprocessor Systems on Chip (MPSoC)	Ines Viskic and Daniel Gajski, "Modeling Process Synchronization in Multiprocessor Systems on Chip (MPSoC)," TR 08-07, May 10th, 2008.
Mission-Critical Multimedia Systems	Kyoungwoo Lee, Aviral Shrivastava, Ilya Issenin, Nikil Dutt, Nalini Venkatasubramanian, "Partially Protected Caches to Reduce Failures due to Soft Errors in Mission-Critical Multimedia Systems," TR 08-06, June 24, 2008.
Custom Co-processors	Jelena Trajkovic and Daniel Gajski, "Generation of Custom Co-processor Structure from C-Code," TR 08-05, June 27, 2008.