

High-Performance Architectures for Brain Circuit Simulation

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Abstract: Humans outperform computers in many natural tasks including vision, natural language processing and many other tasks due to computational principles of the brain. The goal of my thesis is towards development of new generation of high-performance architectures inspired from the understanding of brain circuits. Two main projects have been carried out as a part of this thesis. Firstly, we have developed novel algorithms and architectures for vision applications by analyzing the anatomical and physiological operations of brain circuits. Secondly, we have also developed various brain based simulators operating at different levels of abstraction aided by the recent developments in the computational neuroscience research and availability of low-cost, high performance general purpose graphics processors.

The area of computational neuroscience mainly involves better understanding or reverse engineering of brain by developing software models of various parts of brain. By bridging the area of computer engineering and computational neuroscience it is possible to build next generation of adaptive computing systems that have many characteristics inspired from the brain.

This line of research can solve many challenges associated with building smart and efficient computing systems for futuristic applications in vision, robotics, ambient intelligence etc. But many complex software models of brain circuits are very slow to simulate and use for real-time applications. The focus of my research is to use the engineering and supercomputing principles in order to build faster models of brain using various computational paradigm so that one day we can simulate large-scale brain like networks to solve the hardest problems in computing, namely making computers more intelligent. Interestingly, the National Academy of Engineers (NAE) has also declared that reverse-

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engineering the brain as one of the grand challenges of the 21st century.

We cannot understate the advantages of looking at the ultimate machine (“brain”) for building new kinds of systems. First of all we already know that the human brain is about a million times more energy efficient than a supercomputer of equivalent performance. Secondly, even if we did have an equivalent supercomputer it may still not match the brain’s capability; for instance in the execution of the vision tasks that can be so effortlessly done by a rat or a house fly. If you look beyond the computational principles that typically interest computer engineers, there are many advantages for better understanding of brain in the area of medicine, artificial intelligence, human-computer interaction and much more.

In order to address the above mentioned research goals, I am currently working on the thesis project called BRICS (brain inspired computing systems) at CECS (Center for Embedded Computing System) in University of California, Irvine. My primary advisor in this research is Prof. Nikil Dutt from CECS. This interdisciplinary project also involves active guidance of Prof. Jeffrey Krichmar from the Department of Cognitive Science at University of California, Irvine. In this thesis project, my aim is to develop new computational principles inspired by brain circuitry, and develop computational platforms for simulation of brain circuitry, as well as programming models for algorithms derived from the principles of brain circuitry. Figure 1 shows the different level at which brain architecture can be modeled and analyzed. Our current focus is on neuron circuit and application specific level in Figure 1.

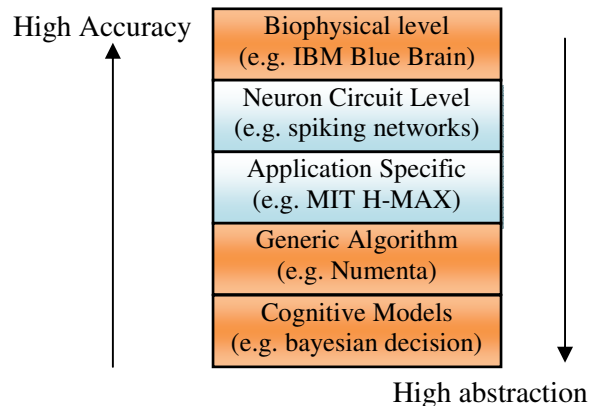


Figure 1: Modeling hierarchy in brain architectures

From a computational perspective, brain inspired algorithms are extremely parallel in nature when compared against conventional algorithms. Hence these brain-inspired algorithms offer both an opportunity, as well as a challenge for effective mapping onto, and simulation using modern multiprocessing platforms. As a part of my research I have investigated the use of several multiprocessing platforms for simulation, including conventional computing clusters, modern high-performance architectures such as the IBM CELL, general purpose graphics processors such as the NVIDIA CUDA platform, and also reconfigurable fabrics using FPGAs.

In the past three years I have been working on many different topics related to brain inspired system. My first work dealt with hardware and parallel processor realization of Basal Ganglia which is an important part of motor control in human brain. We have tried to use the Basal Ganglia based neural network model for different kinds of learning tasks and demonstrated the correlation between the reinforcement based learning algorithm and Basal Ganglia.

Our next work was focused on using a brain inspired algorithm developed by Dartmouth and UCI for object recognition. In my research I proposed a generic framework for analyzing the performance of various parallel models of brain inspired vision algorithm on a cluster of IBM CELL Processors [3]. As a part of this research I investigated simple PC clusters, high-performance/low-cost clusters of PS3 from Sony having IBM CELL processor [4], and also cluster of low-cost FPGA [5].

Currently our focus is on building bottom-up models of brain circuits that takes into account the computation principles of neurons, role of spike frequency and timing in computation. Using the principles of low-level spiking neural networks, our goal is to extend high-level models for object recognition and other applications. As a part of this research, we demonstrated an object recognition algorithm using an array of spiking neural networks simulated on NVIDIA GTX-280 GPU [1]. We also demonstrated a medium scale spiking networks consisting of 100K neurons and 40 Million synapses using CUDA GPUs [2]. We used biologically accurate models of neurons, synaptic connections and also axons for our studies. Based on these results we are planning on simulating larger-scale spiking neural network models having more than 1 million neurons and 1 billion synapses using cluster of high-performance CUDA GPUs. We are beginning to use these large-scale models in building brain-based devices where a suitable brain model running on GPUs is used to control a robot for different tasks in diverse environment.

With tremendous improvements in brain imaging technologies, and other neuroscience related discoveries, harnessing the potential of new high-performance supercomputing platforms for simulation of large scale brain circuits would accelerate the development of new applications and help in understanding the principles of brain circuits.

Referred Conference and Journal Papers

- [1] J. Moorkanikara Nageswaran, Yingxue Wang, Tobi Delbruck, Nikil Dutt, "Computing Spike Based Convolutions on GPUs", *Intl. Symposium on Circuits And Systems (ISCAS)*, 2009 (accepted)
- [2] J. Moorkanikara Nageswaran, Nikil Dutt, Jeffrey L Krichmar, Alex Nicolau, Alex Veidenbaum, "Efficient Simulation of Large-Scale Spiking Neural Networks using Graphics Processors", *Int. Joint Conf. on Neural Networks (IJCNN)*, 2009 (accepted)
- [3] J. Moorkanikara Nageswaran , et al., "Scalable Parallel Implementations of a Brain Derived Vision Algorithm", *Journal of Parallel Programming*, Special issue on Bio/Nano Applications, 2009 (accepted)
- [4] Andrew Felch, J. Moorkanikara Nageswaran , et al., "Accelerating Brain Circuit Simulations of Object Recognition with CELL Processor", *Intl. Workshop on Innovative Architectures (IWIA)*, 2007
- [5] Jeff Furlong, Andrew Felch, J. Moorkanikara Nageswaran , et al., "Novel Brain-Derived Algorithms Scale Linearly with Number of Processing Elements", *Parallel Computing on FPGA (ParaFPGA)*, 2007