Student ID: _____

CS 151
Midterm

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

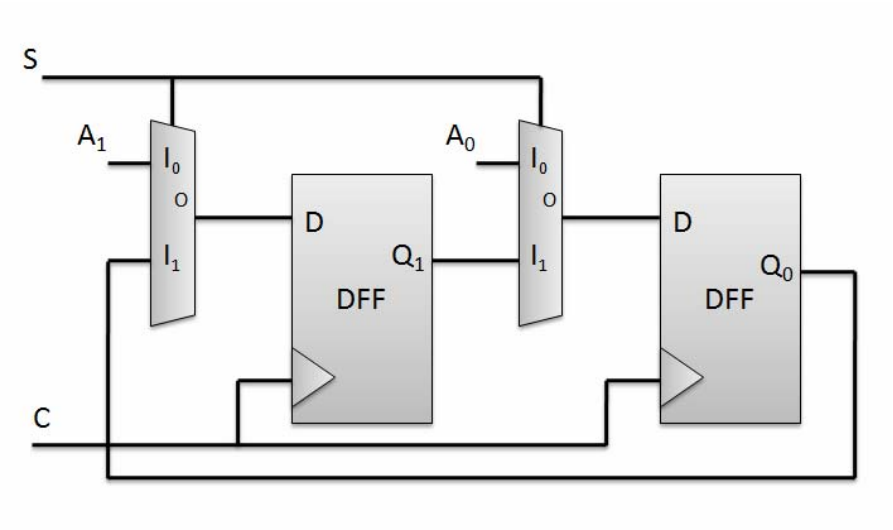
1. Please verify that your paper contains **13 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this midterm are **80 points.**
5. To receive credit you must show your work clearly.
6. **Re-grade requests will not be entertained unless you write clearly.**
7. Calculators are **NOT** allowed.
8. If necessary, state your assumptions clearly

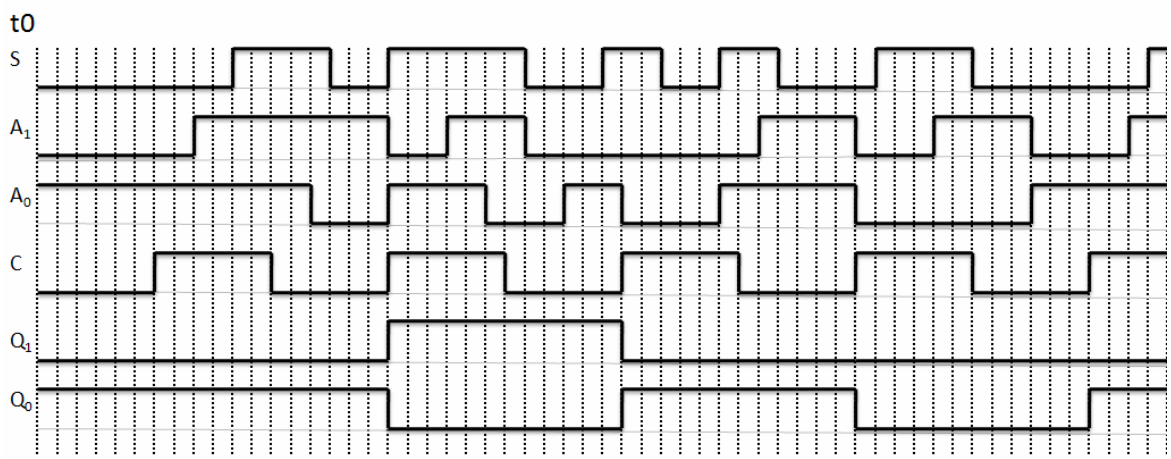
Student ID: _____

Q1: [Sequential Circuit Timing Analysis] [10 points]

The circuit below shows a sequential circuit using D Flip Flops, and Multiplexers. Assuming that $\mathbf{A_1}$, $\mathbf{A_0}$, and **S** are the inputs of the circuit, and $\mathbf{Q_1}$ is 0, $\mathbf{Q_0}$ is 1 when time equals 0 (**t0**), show the timing diagram for Q_1 and Q_0.

NOTE: You can assume that gate delay is negligible.





Student ID: _____

Q2: [ALU] [20 points]

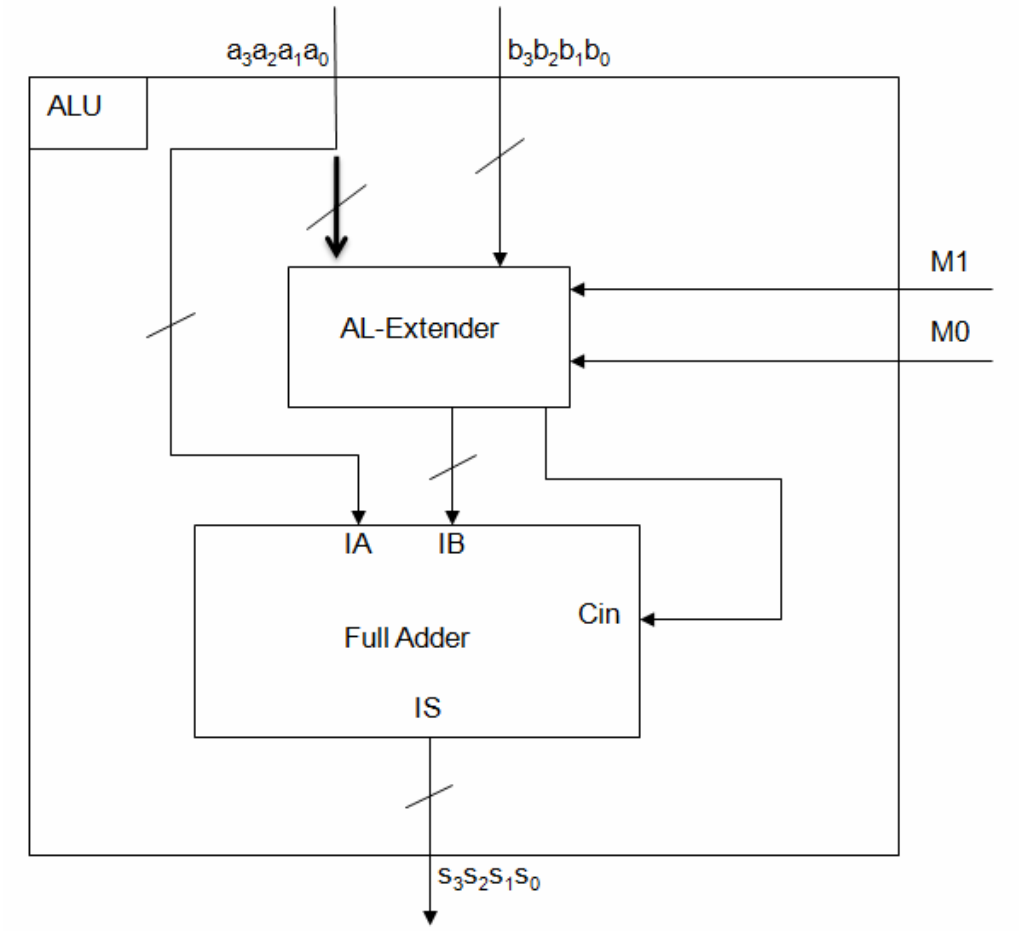
We are going to design a 4-bit Arithmetic Unit (AU) with the following functional table:

M1	M0	Function Name	F(A,B)
0	**0**	**if(A/4==0) add B to A; else subtract B from A**	**if(A/4==0) S = A + B; else S = A – B**
0	**1**	**if(A<B) add A to B times 8; else add A to B divided 4**	**if(A<B) S = A + (B * 8); else S = A + (B / 4)**
1	**0**	**Increment A by 4**	**S = A + 4**
1	**1**	**Add 1 to A+B * 8**	**S = A + (B * 8) + 1**

Both A and B are 4-bit binary unsigned numbers a3a2a1a0 and b3b2b1b0.
M1, M0 are the control inputs to this AU. Although B is the only input register to the AL-Extender unit, if you need to, you can also connect register A to the AL-Extender.

In this question you are required to design the logic inside AL-Extender using JUST Comparators, and Multiplexers if needed.

Hint: Although the inputs and outputs are unsigned numbers, you can use 2's complement arithmetic within the design.



Student ID: _____

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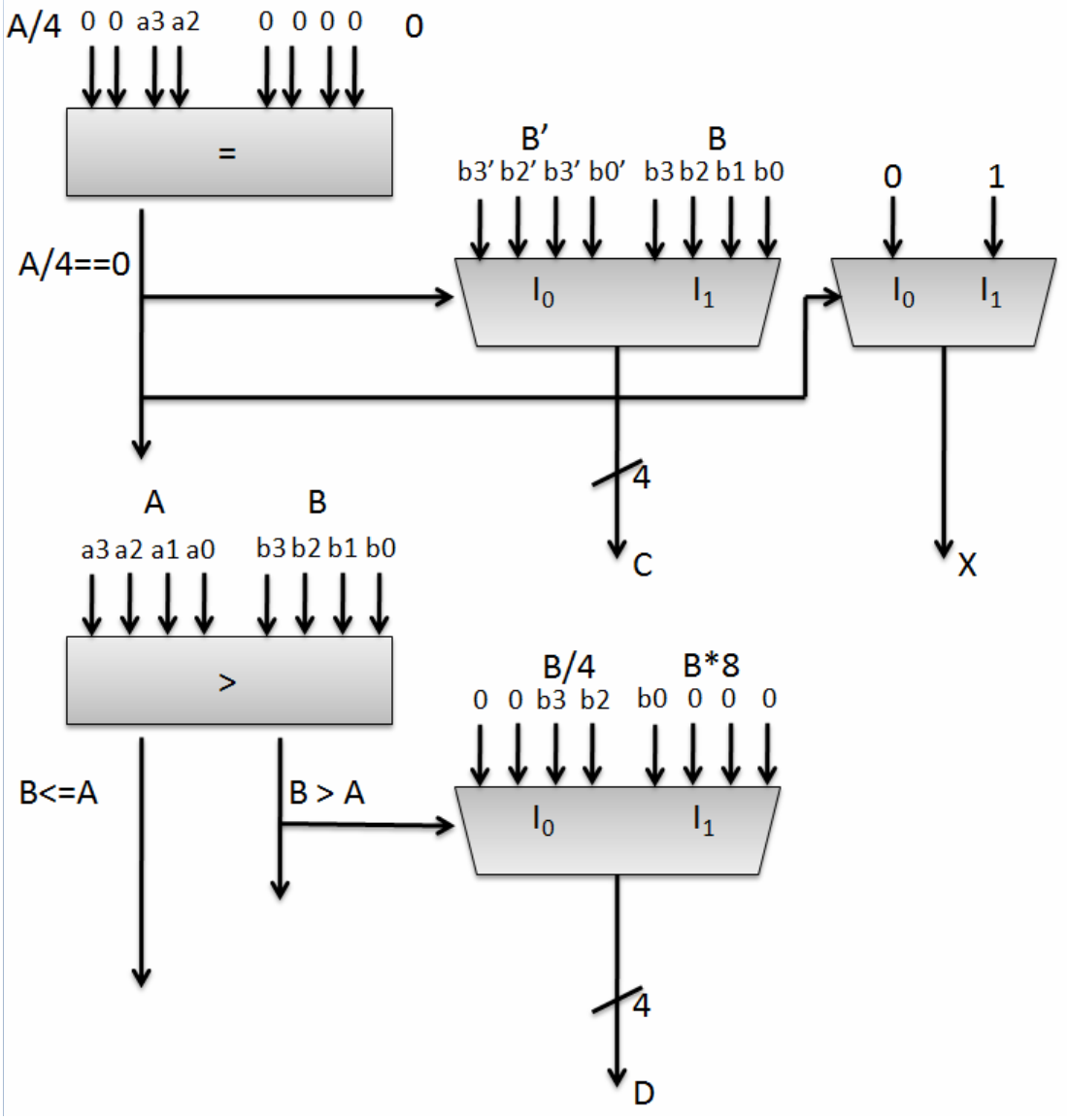

Student ID: _____

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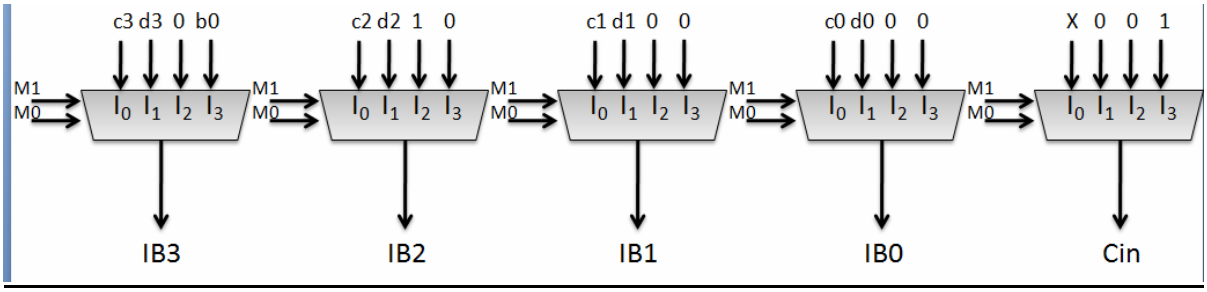

Student ID: _____

Q3: [Counter Application] [15 points]

Using **only a 3-bit up** binary counter, you are going to design a mod-8 counter whose output (denoted by **MOD8**) is 1 when the sequence value mod 8 equals 0, otherwise it outputs a 0. You can use any of the following components (**Specify the bit widths, and name all inputs/outputs**):

1) Adders
2) Shifters
3) Comparators
4) Multiplexers

Make sure you answer both parts A and B.

3a. Using the 3-bit up binary counter, create a counter that generates the following sequence [10 points]:

$2 \rightarrow 4 \rightarrow 6 \rightarrow 8 \rightarrow 10 \rightarrow 12 \rightarrow 14 \rightarrow 16 \rightarrow 2 \rightarrow 4 \ldots..$

For the solution see page 7

Student ID: _____

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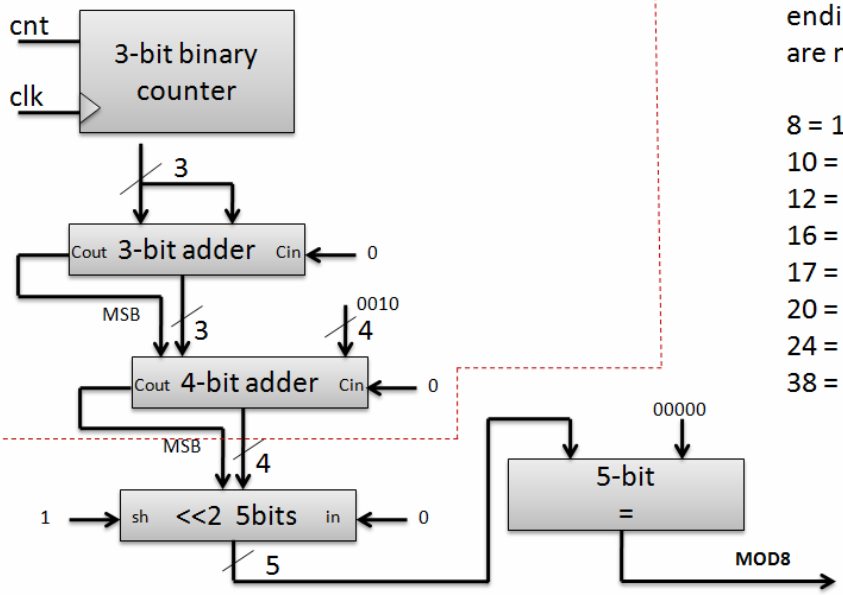
A

3-bit binary counter counts from 0 to 7, and resets
So:

2 = 0 * n + i, i = 2
4 = 1 * n + 2, n = 2
Equation: Counter output = 2 * counter value + 2



B

Mod 8:

8 = 1000

All binary values ending with '000' are mod 8

8 = 10000 yes
10 = 01010 no
12 = 01100 no
16 = 10000 yes
17 = 10001 no
20 = 10100 no
24 = 11000 yes
38 = 11110 no

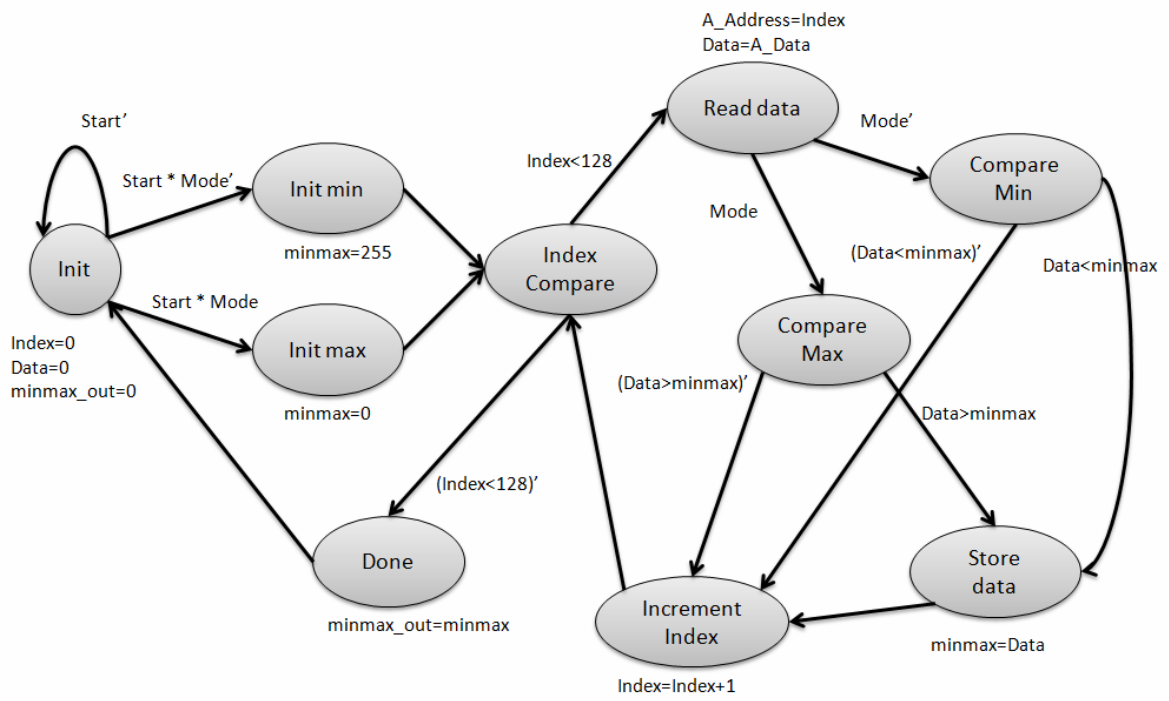
3b. Using the counter designed in part 3a design a mod-8 counter whose output (denoted by MOD8) is 1 when the sequence value mod 8 equals 0, otherwise it outputs a 0. [5 points]

For the solution see page 7

Student ID: _____

Q4: [RTL design] [35 points]

The following high-level state machine has the task of finding either the minimum or the maximum among an array of 128 elements depending on the mode selected (Mode = 0 = find the minimum, and Mode = 1 = find the maximum). A_Data is an 8-bit input, A_Address is an 8-bit output, and minmax_out is the final 8-bit (minimum or maximum) output value. Data and minmax are both 8-bit internal registers. All inputs/outputs are unsigned. The Start input drives the circuit to start the execution of the task. Use this state machine to answer the following questions:



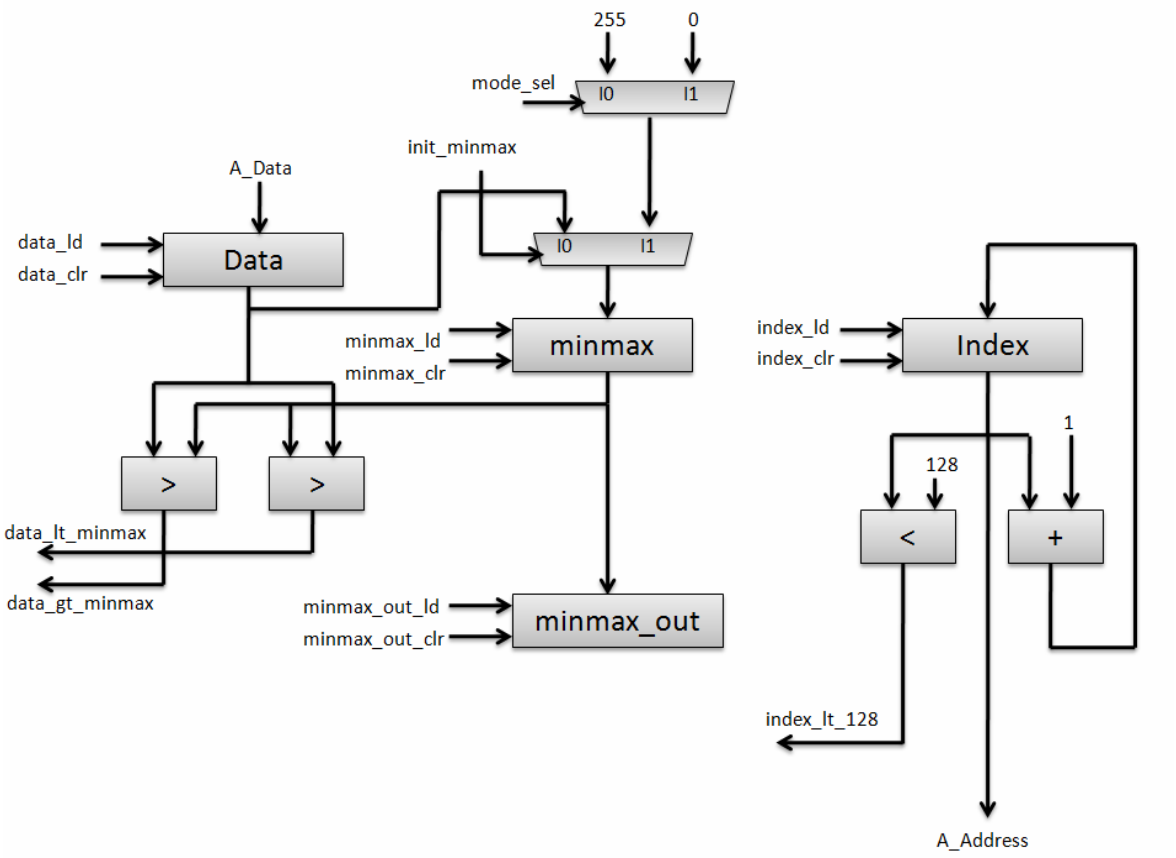
Student ID: _____

4a. Design the data-path for this system. [15 points]

Please note that the initial value for the minmax register depends on the Mode, if the Mode = 0, minmax is initialized to 0, if the Mode = 1, minmax is initialized to (255).
Hint: Your minmax register will have at most 2 inputs.

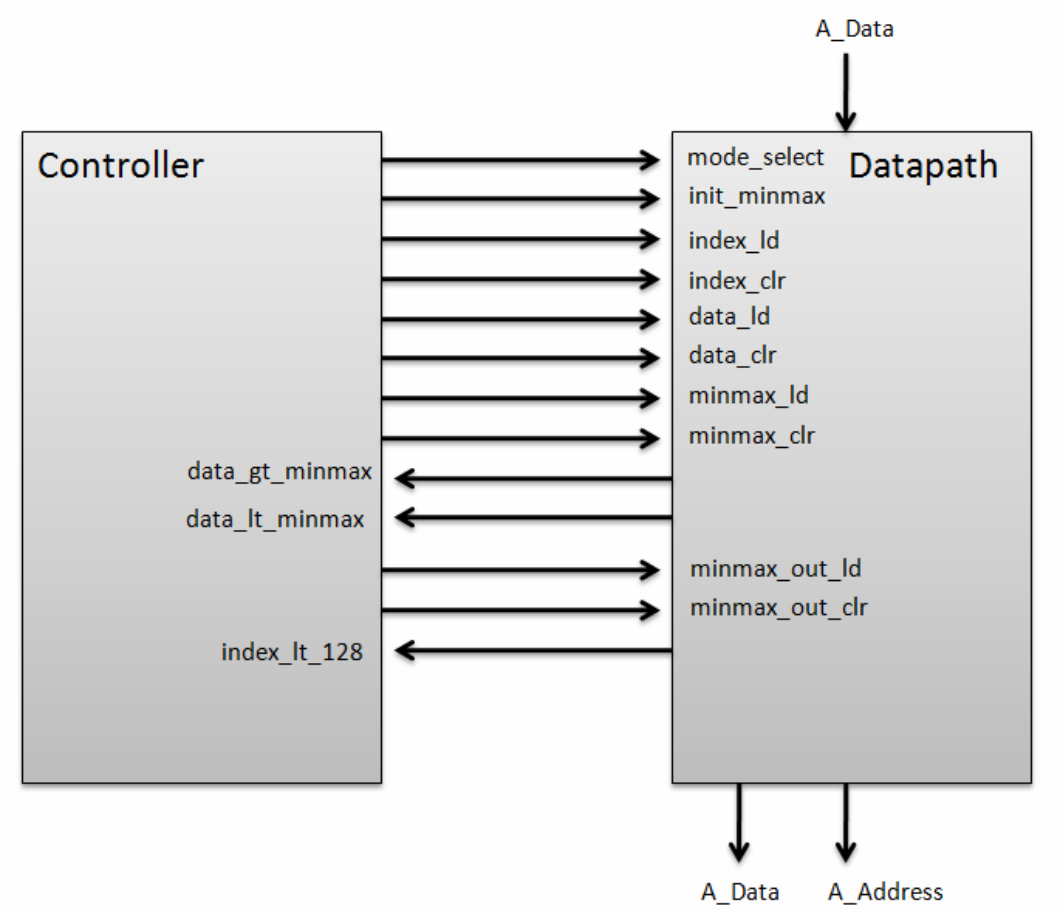
You may use any of the following components:

1) Registers
2) Adders
3) Comparators
4) Multiplexers



Student ID: _____

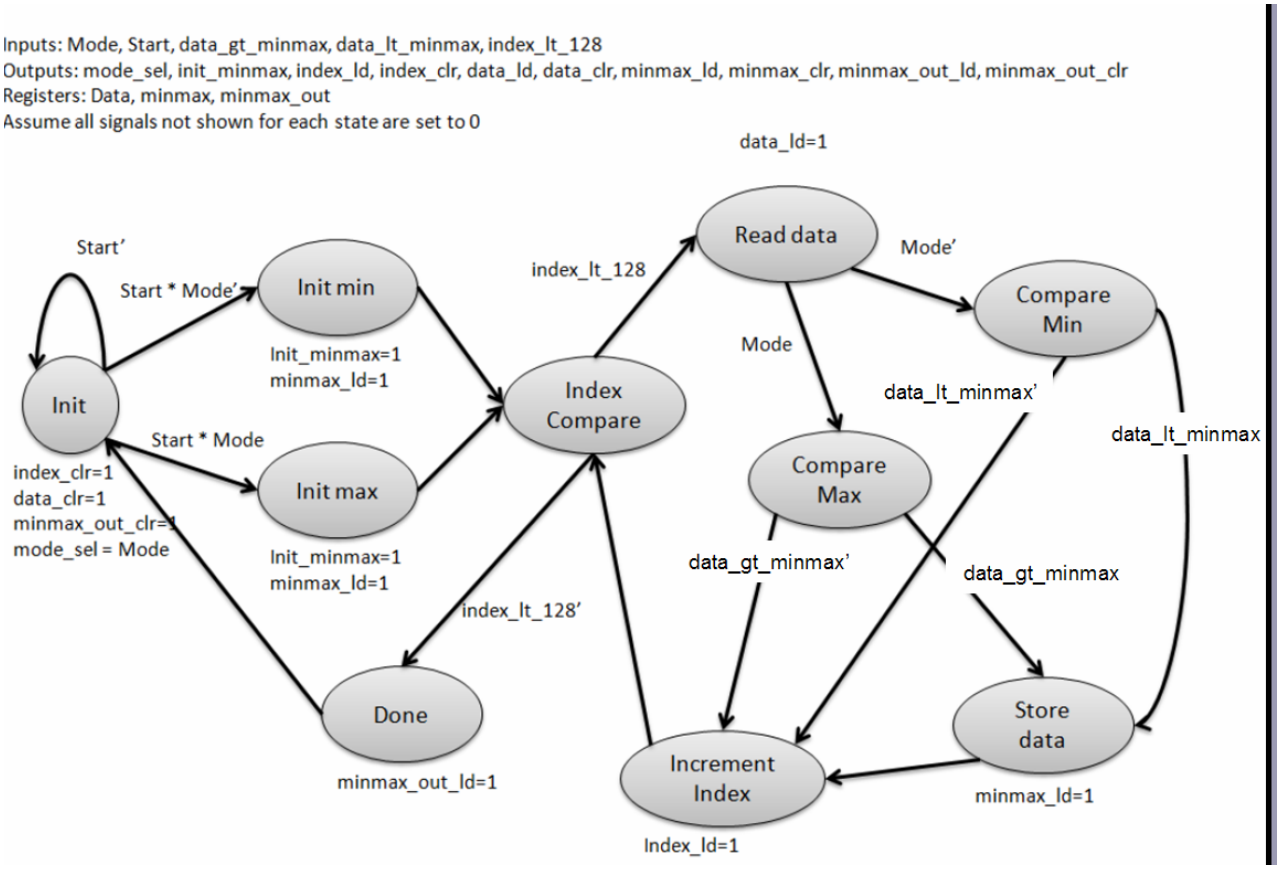
4b. Design the interface of the system and the interface between the controller and the datapath. [5 points]



Student ID: _____

4c. Design the FSM of the controller. [15 points]

HINT: There is no timing issue for this system so you do not have to consider timing issues in designing the controller's FSM.



Student ID: _____

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