

Student ID: _____

CS 151 Quiz 3

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

1. Please verify that your paper contains **8 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this midterm are **60 points**.
5. To receive credit you must show your work clearly.
6. **No re-grades will be entertained if you use a pencil.**
7. Calculators are **NOT** allowed.

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Q1: [FSM Design]

[30 points]

On an intersection there is a traffic light which is initially Red. When a car arrives at the intersection, it triggers the following sequence:

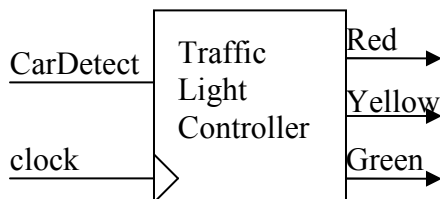
- A)** Traffic light remains Red for 2 cycles,
- B)** Traffic light turns Green for 4 cycles,
- C)** Traffic light turns Yellow for 3 cycles,
- D)** Traffic light returns to Red,

When traffic light is Green if another car is detected at the intersection then the traffic light remains Green for an additional 4 cycles from that instance.

This process is repeated for a maximum of 2 cars when the traffic light is Green.

Assume when the traffic light is yellow, cars pass through the intersection and do not affect the behavior of the traffic light controller:

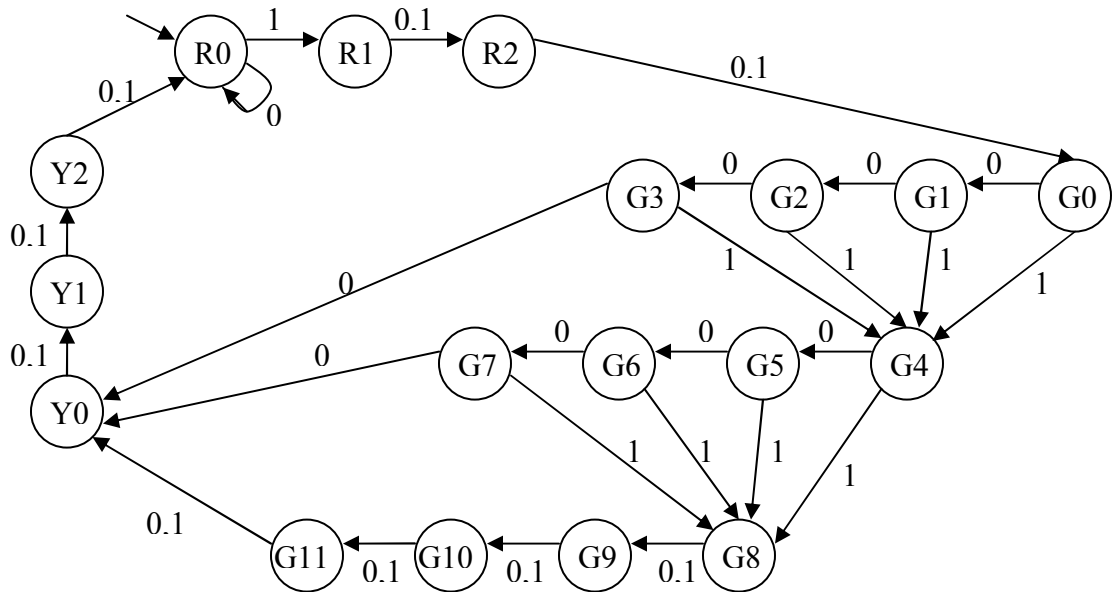
In this question you will design the controller for the traffic light. Assume the output signals of the controller are Green, Yellow and Red signal to the traffic light.



- a. Capture the FSM. (15 points)

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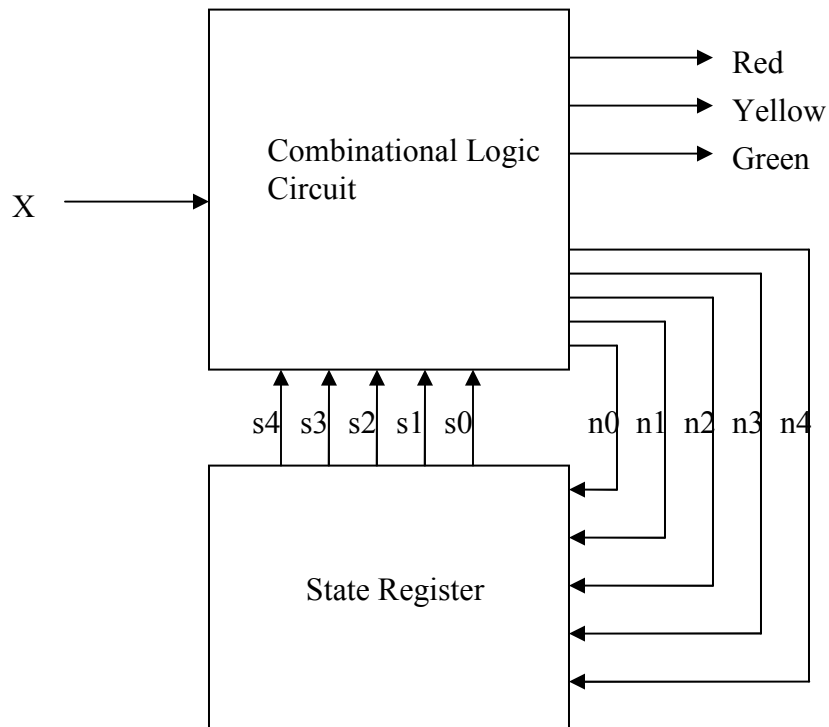
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During Rx states the Red signal should be 1 and Green and Yellow signals are 0.
During Gx states the Green signal is 1 and the others are 0 and finally when we're in
Yx states the Yellow signal is 1 and Green and Red signals are 0.

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b. Create the architecture (3 points)



c. Encode the states (use a simple binary encoding) (2 points)

Answer:

There are 18 states, so we need $\lceil \log_2 18 \rceil = 5$ bits to encode the states. So we will have:

R0 = 00000 R1 = 00001 R2 = 00010

G0 = 00011 G1 = 00100 G2 = 00101 G3 = 00110 G4 = 00111

G5 = 01000 G6 = 01001 G7 = 01010 G8 = 01011 G9 = 01100

G10 = 01101 G11 = 01110

Y0 = 01111 Y1 = 10000 Y2 = 10001

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d. Create the state table (5 points)

Present State					Input	Next State					Output 0	Output 1	Output 2
S4	S3	S2	S1	S0	X	N4	N3	N2	N1	N0	G	Y	R
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	1	0	0	0	0	1	0	0	1
0	0	0	0	1	0	0	0	0	1	0	0	0	1
0	0	0	0	1	1	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	0	0	1	1	0	0	1
0	0	0	1	0	1	0	0	0	1	1	0	0	1
0	0	0	1	1	0	0	0	1	0	0	1	0	0
0	0	0	1	1	1	0	0	1	1	1	1	0	0
0	0	1	0	0	0	0	0	1	0	1	1	0	0
0	0	1	0	0	1	0	0	1	1	1	1	0	0
0	0	1	0	1	0	0	0	1	1	1	1	0	0
0	0	1	0	1	1	0	0	1	1	1	1	0	0
0	0	1	1	0	0	0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	0	1	0	1	1	0	0
0	0	1	1	1	0	0	0	1	1	1	1	0	0
0	0	1	1	1	1	0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	0	1	0	0	1	0	0
0	1	0	0	0	1	0	0	1	0	0	1	0	0
0	1	0	0	1	0	0	0	1	1	1	1	0	0
0	1	0	0	1	1	0	0	1	1	1	1	0	0
0	1	0	1	0	0	0	0	1	0	0	1	0	0
0	1	0	1	0	1	0	0	1	0	0	1	0	0
0	1	0	1	1	0	0	0	1	1	0	1	0	0
0	1	0	1	1	1	0	0	1	1	0	1	0	0
0	1	1	0	0	0	0	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	1	0	0	1	0	0
0	1	1	0	1	0	0	0	1	1	0	1	0	0
0	1	1	0	1	1	0	0	1	1	0	1	0	0
0	1	1	1	0	0	0	0	1	1	1	1	0	0
0	1	1	1	0	1	0	0	1	1	1	1	0	0
0	1	1	1	1	0	0	0	1	1	1	1	0	0
0	1	1	1	1	1	0	0	1	1	1	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	1	0	0	0	0	1	0	1	0
1	0	0	0	1	0	0	0	0	0	0	0	1	0
1	0	0	0	1	1	0	0	0	0	0	0	1	0

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- e. Implement the combinational logic (no need to draw the gates, just write the equations) (5 points)

Answer:

$$\text{Red} = s_4's_3's_2's_1's_0' + s_4's_3's_2's_1's_0 + s_4's_3's_2's_1s_0'$$

$$\text{Yellow} = s_4's_3s_2s_1s_0 + s_4s_3's_2's_1's_0' + s_4s_3's_2's_1's_0$$

$$\begin{aligned} \text{Green} = & s_4's_3's_2's_1s_0 + s_4's_3's_2s_1's_0' + s_4's_3's_2's_1's_0 + s_4's_3's_2s_1s_0' + s_4's_3's_2s_1s_0 + \\ & s_4's_3s_2's_1's_0' + s_4's_3s_2's_1's_0 + s_4's_3s_2's_1s_0' + s_4's_3s_2's_1s_0 + s_4's_3s_2s_1's_0' + s_4's_3s_2s_1's_0 + \\ & s_4's_3s_2s_1s_0' \end{aligned}$$

$$N_4 = s_4's_3s_2s_1s_0X' + s_4's_3s_2s_1s_0X + s_4s_3's_2's_1's_0'X' + s_4s_3's_2's_1's_0'X$$

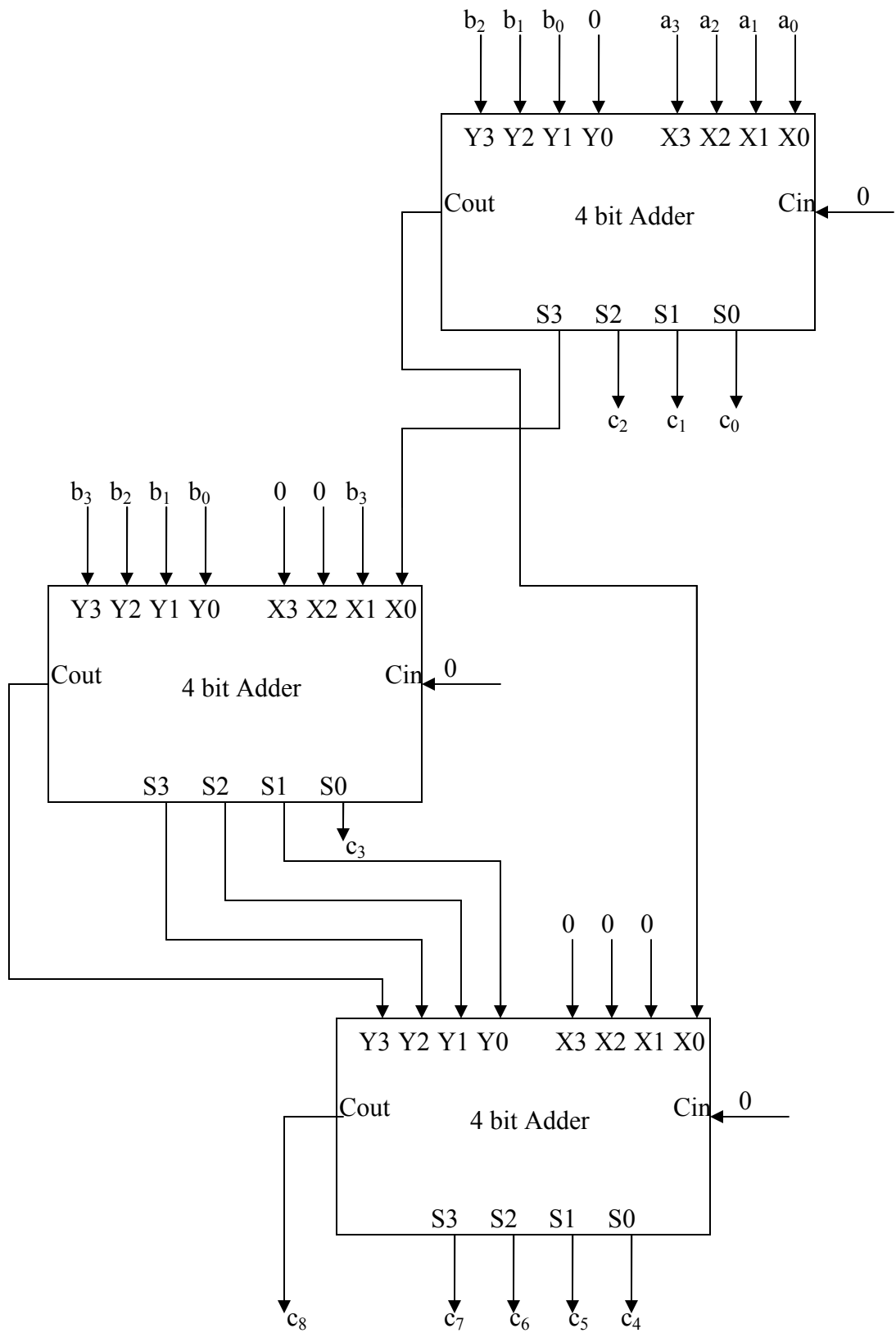
$$\begin{aligned} N_3 = & s_4's_3's_2s_1s_0'X' + s_4's_3's_2s_1s_0X' + s_4's_3's_2s_1s_0X + s_4's_3s_2's_1's_0'X' + s_4's_3s_2's_1's_0'X + \\ & s_4's_3s_2's_1's_0X' + s_4's_3s_2's_1's_0X + s_4's_3s_2's_1s_0'X' + s_4's_3s_2's_1s_0'X + s_4's_3s_2's_1s_0X' + \\ & s_4's_3s_2's_1s_0X + s_4's_3s_2s_1's_0'X' + s_4's_3s_2s_1's_0'X + s_4's_3s_2s_1's_0X' + s_4's_3s_2s_1's_0X + \\ & s_4's_3s_2s_1s_0'X' + s_4's_3s_2s_1s_0'X \end{aligned}$$

$$\begin{aligned} N_2 = & s_4's_3's_2's_1s_0X' + s_4's_3's_2's_1s_0X + s_4's_3's_2s_1's_0'X' + s_4's_3's_2s_1's_0'X + s_4's_3's_2s_1's_0X' + \\ & + s_4's_3's_2s_1's_0X + s_4's_3's_2s_1s_0'X' + s_4's_3's_2s_1s_0'X + s_4's_3s_2's_1s_0'X' + s_4's_3s_2's_1s_0X' + \\ & s_4's_3s_2's_1s_0X + s_4's_3s_2s_1's_0'X' + s_4's_3s_2s_1's_0X + s_4's_3s_2s_1's_0X' + s_4's_3s_2s_1's_0X + \\ & s_4's_3s_2s_1s_0'X' + s_4's_3s_2s_1s_0'X \end{aligned}$$

$$\begin{aligned} N_1 = & s_4's_3's_2's_1's_0X' + s_4's_3's_2's_1's_0X + s_4's_3's_2's_1s_0'X' + s_4's_3's_2's_1s_0'X + s_4's_3's_2's_1s_0X + \\ & + s_4's_3's_2s_1's_0'X + s_4's_3's_2s_1's_0X' + s_4's_3's_2s_1's_0X + s_4's_3's_2s_1s_0'X' + s_4's_3's_2s_1s_0'X + \\ & s_4's_3's_2s_1s_0X + s_4's_3s_2's_1's_0'X' + s_4's_3s_2's_1's_0X' + s_4's_3s_2's_1's_0X + s_4's_3s_2's_1s_0'X' + \\ & s_4's_3s_2's_1s_0'X + s_4's_3s_2s_1's_0X' + s_4's_3s_2s_1's_0X + s_4's_3s_2s_1s_0'X' + s_4's_3s_2s_1s_0'X \end{aligned}$$

$$\begin{aligned} N_0 = & s_4's_3's_2's_1's_0'X + s_4's_3's_2's_1s_0'X' + s_4's_3's_2's_1s_0'X + s_4's_3's_2's_1s_0X + s_4's_3's_2s_1's_0'X' + \\ & + s_4's_3's_2s_1's_0'X + s_4's_3's_2s_1's_0X + s_4's_3's_2s_1s_0'X' + s_4's_3's_2s_1s_0'X + s_4's_3's_2s_1s_0X + \\ & s_4's_3s_2's_1's_0'X' + s_4's_3s_2's_1's_0'X + s_4's_3s_2's_1's_0X + s_4's_3s_2's_1s_0'X' + s_4's_3s_2's_1s_0'X + \\ & s_4's_3s_2s_1's_0'X' + s_4's_3s_2s_1's_0'X + s_4's_3s_2s_1s_0'X' + s_4's_3s_2s_1s_0'X + s_4s_3's_2's_1's_0'X' + \\ & s_4s_3's_2's_1's_0'X \end{aligned}$$

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Q3: [Counter usage]

[15 points]

Using only one 3-bit binary counter and minimum number of components listed below; design a counter that generates the following sequence repeatedly:

3 → 6 → 9 → 12 → 15 → 18 → 21 → 24 → 3

- a) Shifter
- b) Adder
- c) Subtractor
- d) Comparator

Answer:

As can be seen the sequence is $3 \cdot X + 3$ where X , ranges between 0 and 7. We can design the component as following:

