ICS 151
Quiz 5

Name : ______________________ , ______________________
       (Last Name)          (First Name)

Student ID : ________________
Signature : ________________

Instructions:

1. Please verify that your paper contains 4 pages including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is closed book. No notes or other materials are permitted.
4. Total credits of this quiz are 50 points.
5. To receive credit you must show your work clearly.
6. No re-grades will be entertained if you use a pencil.
7. Calculators are NOT allowed.
Q1: Function Minimization

Consider function \( F \) with the following equation:

\[
F(a, b, c, d) = a'b'c'd' + a'bc'd' + a'bc'd + abcd + abcd' + ab'cd' + ab'c'd'
\]

Assuming that \( abcd = 0011 \) never happens in the input (so you can regard it as don’t care situation):

a. Fill the following K-map table (5 points)

```
   cd       00   01   11   10
   ab
   00   m0   0   X   m3   0
   01   m4   0   0   m7   0
   11   0     0   m15  1   1
   10   m8   0   m11  1   1
```

b. Identify Prime Implicants and Essential Prime Implicants. (15 points)

Prime Implicants:
\[ m_4 + m_5 = a'bc' \]
\[ m_0 + m_4 = a'c'd' \]
\[ m_0 + m_8 = b'c'd' \]
\[ m_8 + m_0 = ab'd' \]

Essential Prime Implicants:
\[ m_4 + m_5 = a'bc' \]
\[ m_{14} + m_{15} = abc \]

c. Using the K-map table in 1(a), write the minimized equation for function F. (10 points)

Minimized equation = Essential Prime Implicants, +
non-Essential Prime Implicants

\[ = \left[ (m_4 + m_5) + (m_{14} + m_{15}) \right] + \]
\[ \left[ (m_4 + m_0) + (m_8 + m_0) \right] \]
\[ = a'bc' + abc + a'c'd' + ab'd' \]
Q2: Size-Delay trade off

Show the trade-off in delay vs. size for the circuit representing function $F$.

$F(a,b,c,d,e,f) = abcd + cdef + abe$

You can use the following gate library showing costs for different gates:

<table>
<thead>
<tr>
<th>Gate</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-input AND</td>
<td>4</td>
</tr>
<tr>
<td>3-input AND</td>
<td>6</td>
</tr>
<tr>
<td>2-input OR</td>
<td>4</td>
</tr>
<tr>
<td>3-input OR</td>
<td>6</td>
</tr>
</tbody>
</table>

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**Diagram 1:**
- $cd(ab+ef)+abe$
- Delay: 4
- Size: 28

**Diagram 2:**
- $d(abc+cef)+abe$
- Delay: 3
- Size: 32