

Student ID: _____

CS 151 Quiz 4

Name : _____ , _____
(Last Name) (First Name)

Student ID : _____

Signature : _____

Instructions:

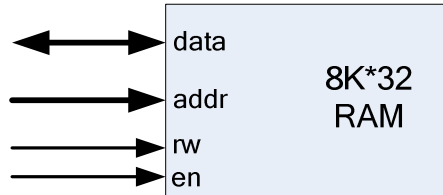
1. Please verify that your paper contains **9 pages** including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is **closed book**. No notes or other materials are permitted.
4. Total credits of this quiz are **50 points**.
5. To receive credit you must show your work clearly.
6. Calculators are **NOT** allowed.

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Q1 [Memory Design]

[10 points]

Design a 16K*64-bit RAM using 8K*32-bit RAM modules shown below.



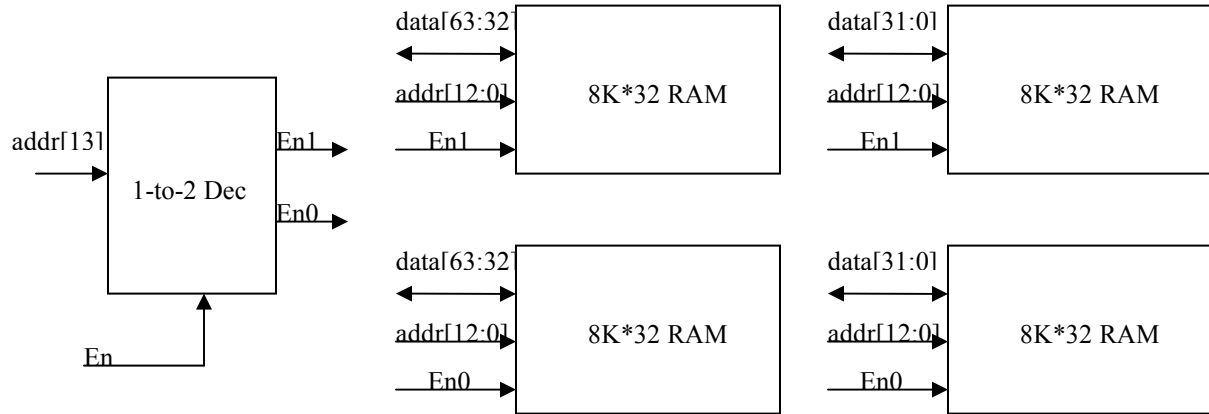
8K*16-bit RAM Module

Use a minimum number of the following logic components in your design (*no other components may be used for this design*):

- 1) Priority Encoder
- 2) Decoder
- 3) Multiplexer

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NOTE: All the $8K*16$ modules share the same line for rw , so that input is not shown in the solution.

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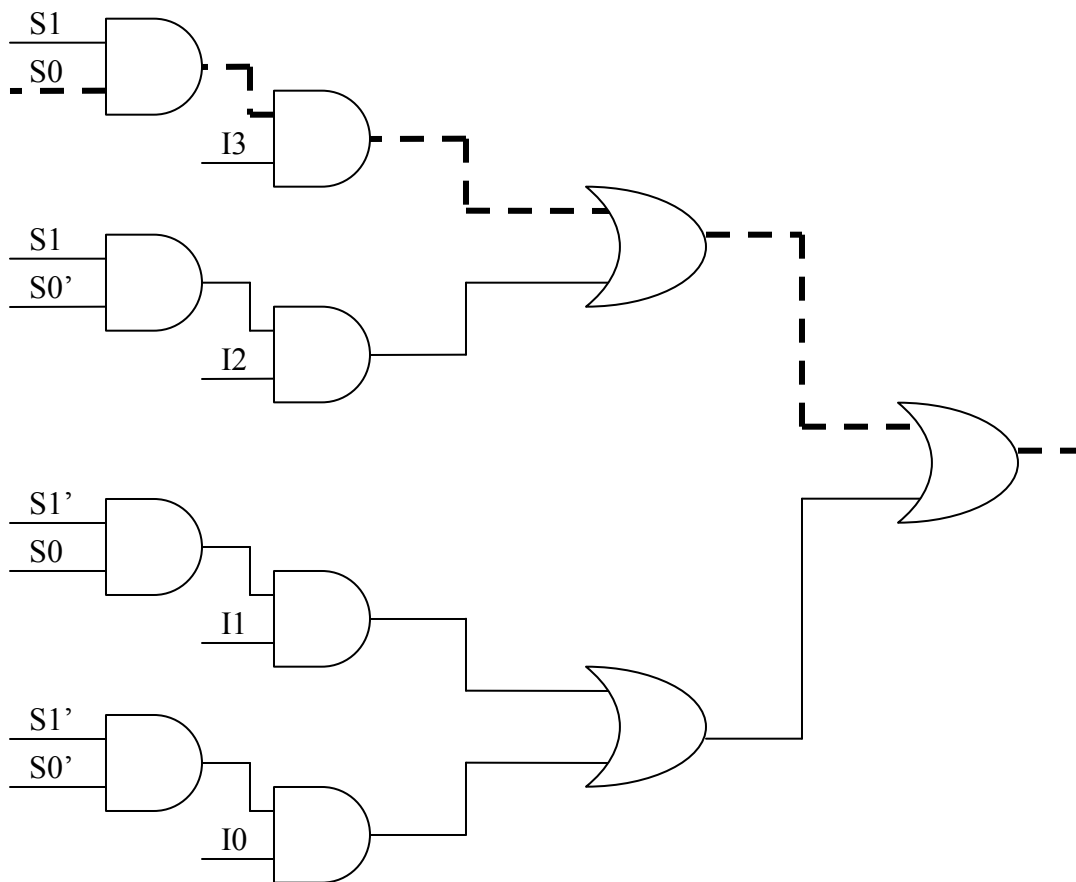
Q2 [Critical Path Delay Calculation]

[15 points]

Assume that you can use only 2-input gates with a gate delay of 2ns and inverters with negligible delay.

a. Determine the critical path delay of a 4-to-1 MUX **built using only 2-input gates and inverters.** [6 points]

The structure of a 4-to-1 MUX is shown below. The critical path is shown using a dashed line.



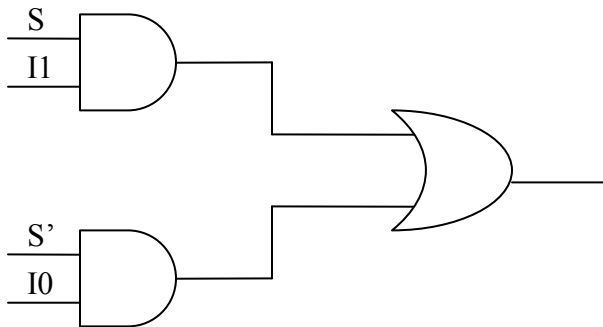
The critical path delay is equal to 4 gate delays which is equal to 8ns.

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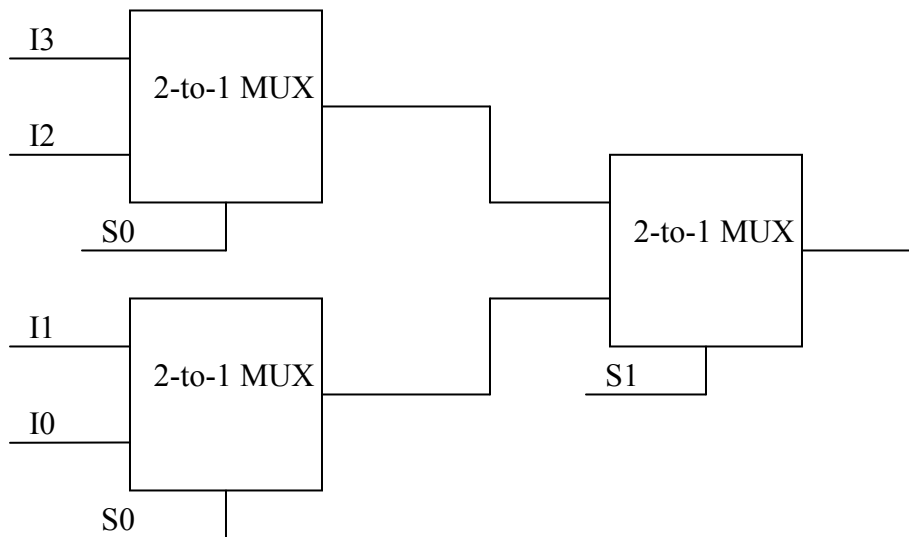
b. Determine the critical path delay of a 4-to-1 MUX **built using 2-to-1 MUX components that are in turn built using 2-input gates and inverters [9 points]**

(HINT: You should first implement a 4-to-1 MUX using 2-to-1 MUXes and then determine the critical path delay of the circuit)

The structure of a 2-to-1 MUX is shown below:



A 4-to-1 MUX can be built using 2-to-1 MUXes in the following way:



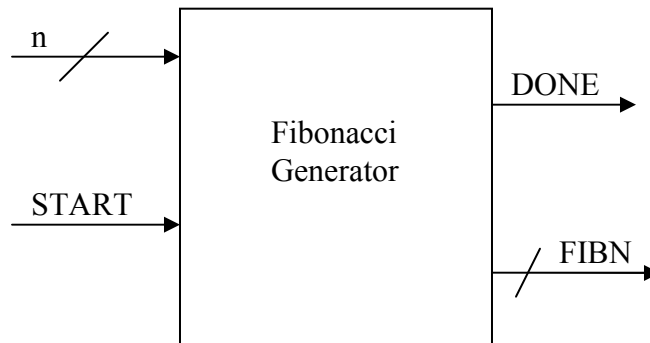
In this design the critical path is still 4 gate delays which is equal to 8 ns.

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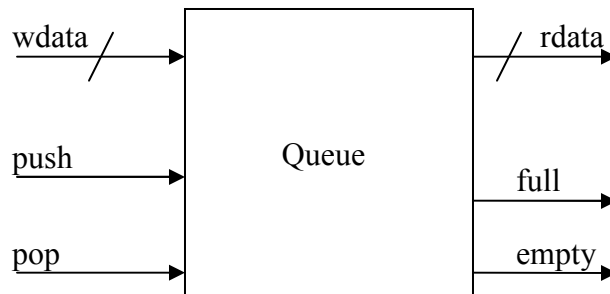
Q3 [RTL Design-Queue Operation]

[25 points]

Design a circuit which takes as an input an integer number n (in the form of a 4 bit unsigned binary number) and computes the n th number in the Fibonacci sequence as the output FIBN. A START signal begins the operation and a DONE signal is asserted when the Fibonacci number is outputted on FIBN, as shown below:



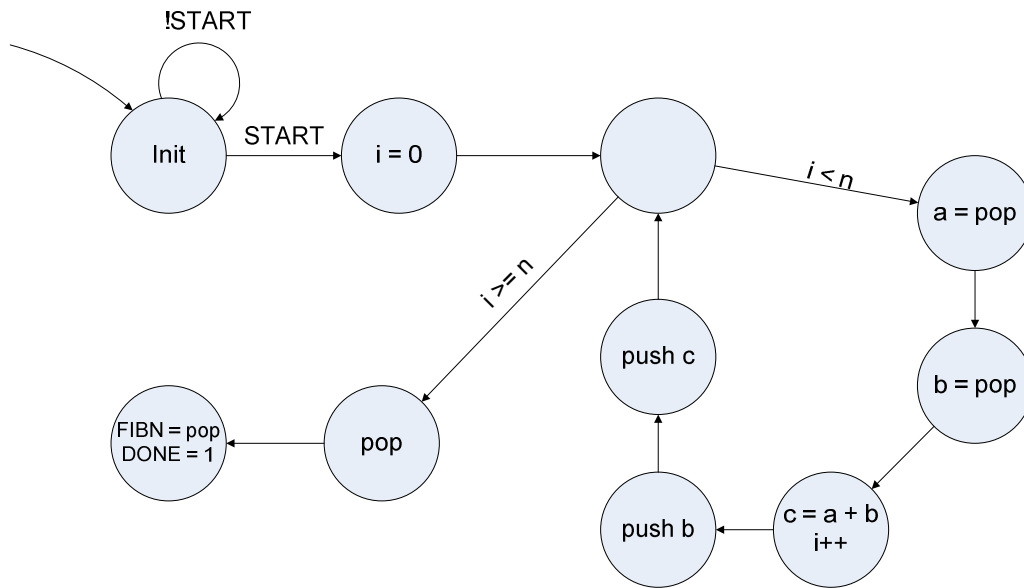
The computation of FIBN should use a queue as shown below. Assume that the first two numbers of Fibonacci sequence are already inserted in the queue, i.e., when you pop the queue the first two times, you will get Fib (0) first and Fib (1) next.



NOTE: n th number in Fibonacci sequence is calculated as following:
 $Fib(n) = Fib(n-1) + Fib(n-2)$

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a) Draw the high-level state machine for this circuit. [10 points]



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b) Draw the data-path. [15 points]

