Instructions:

1. Please verify that your paper contains 5 pages including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is closed book. No notes or other materials are permitted.
4. Total credits of this quiz are 35 points.
5. To receive credit you must show your work clearly.
6. No re-grades will be entertained if you use a pencil.
7. Calculators are NOT allowed.
Q1: [Mux/Decoder application] [15 points]

For function $F(x,y,z) = x'y + x'y'z + x'yz' + xy'z$:

(a) Implement $F$ by means of a 4-to-1 multiplexer (8 points)

(HINT: You can use NOT gates to invert the input to the MUX)
(b) A 3-to-8 decoder (7 points)
Q2: [Latch analysis] [10 points]

Shown below is a NAND implementation of gated D-latch:

The timing diagrams of D and C are shown below. Show the timing diagram for Q and Q': (Assume that Q=0 at t0 and there is no gate delay)

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
<th>Q</th>
<th>Q'</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>Q_{prev}</td>
<td>Q'_{prev}</td>
</tr>
</tbody>
</table>
Q3: [FSM design] [10 points]

We want to design a binary up/down modulo-4 counter. A counter has an input “u”. A modulo-4 counter counts from 0 to 3 and then it starts from “0” (0 → 1 → 2 → 3 → 0 → 1…). When u = “1”, the counter counts up from current value and when u = “0”, the counters counts down from current value (3 → 2 → 1 → 0 → 3 → 2…) and so on.

![Diagram of a modulo-4 counter with inputs u and clk, outputs Q0 and Q1.]

Show the value of output for the following given values for “u”

| u: | 1 → 1 → 1 → 1 → 0 → 0 → 1 → 1 → 0 |
| Q₀Q₁: | 00 → 01 → 10 → 11 → 10 → 01 → 10 → 11 → 10 |
|     | 2 → 3 → 2 → 1 → 2 → 3 → 2 |

Design the FSM for this counter.

The FSM is shown on the next page.