

6.26

$$G_i = a_i b_i, P_i = a_i \text{ xor } b_i$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 G_0 + P_1 P_0 c_0$$

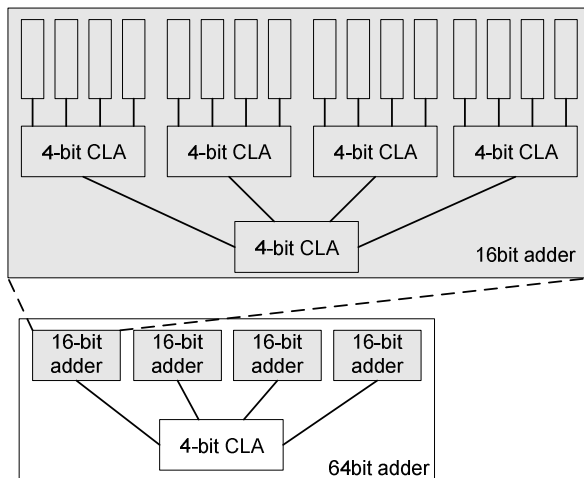
$$c_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0$$

$$c_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0$$

$$a = 11 = 1011, b = 7 = 0111$$

G <sub>0</sub>	1·1 = 1	P <sub>0</sub>	1 xor 1 = 0	c <sub>1</sub>	1 + 0·0 = 1
G <sub>1</sub>	1·1 = 1	P <sub>1</sub>	1 xor 1 = 0	c <sub>2</sub>	1 + 0·1 + 0·0·0 = 1
G <sub>2</sub>	0·1 = 0	P <sub>2</sub>	0 xor 1 = 1	c <sub>3</sub>	0 + 1·1 + 1·0·1 + 1·0·0·0 = 1
G <sub>3</sub>	1·0 = 0	P <sub>3</sub>	1 xor 0 = 1	c <sub>4</sub>	0 + 1·0 + 1·1·1 + 1·1·0·1 + 1·1·0·0·0 = 1

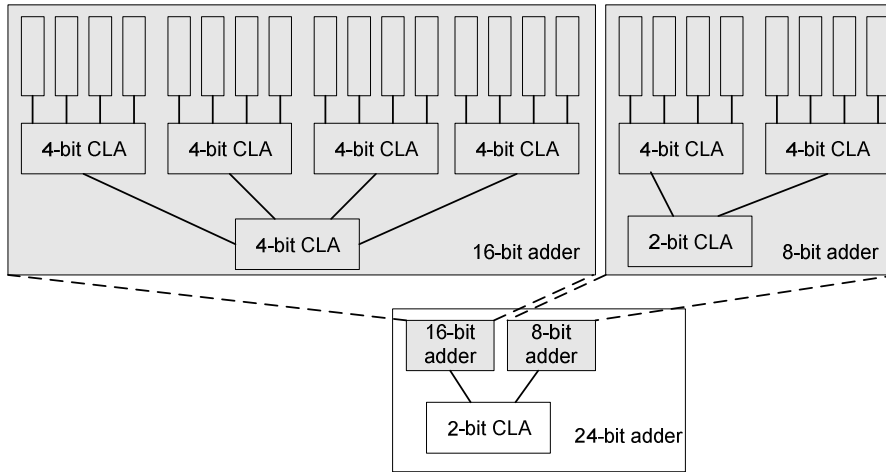
6.29



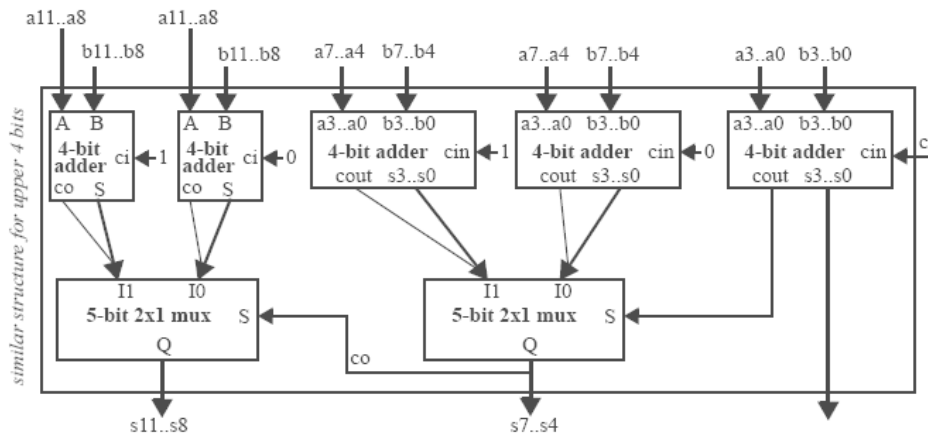
delay of 64-bit hierarchical carry-lookahead adder :  $4 * 2 = 8$ , gate delay

delay of 64-bit carry-ripple adder :  $64 * 2 = 128$ , 128 gate delay

6.30

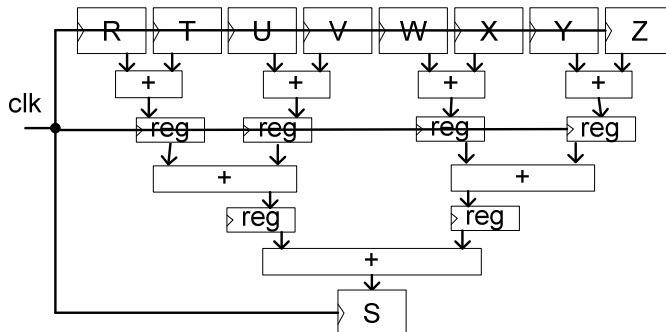


6.31

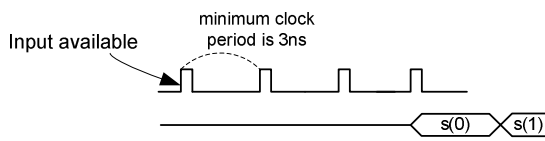


6.32

(a)



(b) assume that delay adder is 3ns.



6.33

in case of 6.94, the minimum clock period must be 9ns.

in case of 6.32, the minimum clock period must be 3ns.

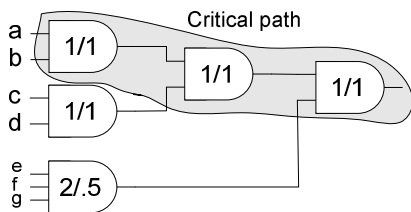
Therefore, pipelined version is three times faster.

6.34

latency : 9ns

throughput : 1 sample every 3 ns

6.44



6.45

