

Nodari Sitchinava

Curriculum Vitae

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Research Interests

Computational models and algorithms for multi-core architectures, parallel external memory and cache-oblivious algorithms, I/O efficient algorithms, geometric and graph algorithms

Education

- 2009 Ph.D. (Computer Science), *University of California, Irvine*
Thesis: “Parallel external memory model and algorithms for multicore architectures”
Advisor: Michael T. Goodrich
- 2003 M.Eng. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*
Thesis: “Dynamic scan chains – a novel architecture to lower the cost of VLSI test”
Advisors: Rohit Kapur and Daniel A. Spielman
- 2002 S.B. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*

Awards and Achievements

- GSR/TA Fellowship, University of California, Irvine 2004 – 2005
- Freedom Support Act Future Leaders Exchange (FSA/FLEX) program scholarship 1997 – 1998
- First and third place medals in regional math and physics competitions, Broken Bow, OK 1998
- Finalist of The National Olympiad in Informatics, Tbilisi, Republic of Georgia 1996, 1997

Research Experience

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| Karlsruhe Institute of Technology <i>Postdoctoral Researcher</i> (Host: Prof. Peter Sanders) | Karlsruhe, GERMANY Sept. 2011 – present |
| MADALGO, University of Aarhus <i>Postdoctoral Researcher</i> (Host: Prof. Lars Arge) | Aarhus, DENMARK Sept. 2009 – Sept. 2011 |
| University of California, Irvine <i>Graduate Student Researcher</i> (Advisor: Prof. Michael T. Goodrich) | Irvine, CA Sept. 2005 – Sept. 2009 |
| Dalhousie University <i>Visiting Student Researcher</i> (Host: Prof. Norbert Zeh) | Halifax, NS, CANADA Fall 2008 |
| MADALGO, University of Aarhus <i>Visiting Student Researcher</i> (Host: Prof. Lars Arge) | Aarhus, DENMARK Summer 2008 |
| MADALGO, University of Aarhus <i>Visting Student Researcher</i> (Host: Prof. Lars Arge) | Aarhus, DENMARK Summer 2007 |
| Synopsys, Inc. <i>Research & Development Engineer in VLSI Test R&D Group</i> | Mountain View, CA Sept. 2003 – Sept. 2004 |
| Synopsys, Inc. <i>Research Internship in VLSI Test R&D Group</i> | Mountain View, CA Summers 2000, 2001; June – Dec. 2002 |

Teaching Experience

- Guest Lecturer, MADALGO, Aarhus University* Spring 2011
 Graduate course “I/O Algorithms” by Prof. Lars Arge.
- Co-Lecturer, MADALGO, University of Aarhus* Spring 2010
 Graduate course “I/O-efficient graph algorithms”. Together with Prof. Norbert Zeh and Dr. Deepak Ajwani.
- Co-Lecturer, MADALGO, University of Aarhus* Summer 2008
 Summer school on cache-oblivious algorithms. Together with Professors Gerth Brodal, Erik Demaine and Norbert Zeh. Attended by 60 faculty, graduate students and post-docs.
- Guest Lecturer, UC Irvine* Spring 2008
 Graduate course ICS 261 “Data structures” by Prof. David Eppstein.
- Teaching Assistant, UC Irvine* Summer 2007
 ICS 161 “Design and analysis of algorithms” by Prof. Daniel Hirschberg.
- Teaching Assistant, UC Irvine* Spring 2005
 ICS 161 “Design and analysis of algorithms” by Prof. David Eppstein.
- Teaching Assistant, UC Irvine* Winter 2005
 ICS H23 “Honors introduction to computer science III” by Prof. Sandy Irani.
- Teaching Assistant, Massachusetts Institute of Technology* Spring 2003
 6.045 “Automata, computability and complexity” by Prof. Ronald Rivest.

Publications

1. Refereed Conference Publications

- [C-1] M.T. Goodrich, N. Sitchinava, Q. Zhang. Sorting, searching and simulation in the MapReduce framework. In *Proceedings of the 22nd International Symposium on Algorithms and Computation (ISAAC)*, 2011.
- [C-2] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal Distribution Sweeping on Private-Cache Chip Multiprocessors. In *Proceedings of the 26th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, 2011.
- [C-3] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. In *Proceedings of the 18th European Symposium on Algorithms (ESA)*, 2010.
- [C-4] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory graph algorithms. In *Proceedings of the 25th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, 2010.
- [C-5] L. Arge, M.T. Goodrich, M. Nelson, N. Sitchinava. Fundamental parallel algorithms for private-cache chip multiprocessors. In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 197-206, 2008.
- [C-6] D. Eppstein, M.T. Goodrich, N. Sitchinava. Guard placement for efficient point-in-polygon proofs. In *Proceedings of the 23rd Annual ACM Symposium on Computational Geometry (SoCG)*, pages 27-36, 2007.
- [C-7] N. Sitchinava, S. Samaranayake, R. Kapur, E. Gizdarski, F. Neuveux, T.W. Williams. Changing scan enable during shift. In *Proceedings of the 22nd IEEE VLSI Test Symposium (VTS)*, pages 73-78, 2004.
- [C-8] S. Samaranayake, E. Gizdarski, N. Sitchinava, F. Neuveux, R. Kapur, T.W. Williams. A reconfigurable shared scan-in architecture. In *Proceedings of the 21st IEEE VLSI Test Symposium (VTS)*, pages 9-14, 2003.

2. Journal Publications

- [J-1] S. Samaranayake, N. Sitchinava, R. Kapur, M. Amin, T.W. Williams. Dynamic Scan: driving down the cost of test. *IEEE Computer* 35(10): 63-68 (2002).

3. Patents

- [P-1] R. Kapur, N. Sitchinava, S. Samaranayake, E. Gizdarski, F. Neuveux, S. Duggirala, T.W. Williams. Dynamically reconfigurable shared scan-in test architecture. US Patents 7,836,368, 7,836,367, 7,774,663, 7,743,299, 7,596,733, 7,418,640.

4. Refereed Workshop Presentations

- [W-1] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2011.
- [W-2] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2010.
- [W-3] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory model. *Workshop on Theory and Many-Cores (T&MC)*, 2009.
- [W-4] N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams. Dynamically reconfigurable shared scan-in architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2004.
- [W-5] N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams, D. Spielman. A segment identification algorithms for a dynamic scan architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2003.
- [W-6] N. Sitchinava, S. Samaranayake, R. Kapur, M. Amin, T.W. Williams. DFT – ATE solution to lower the cost of test. *IEEE Workshop on Test Resource Partitioning*, 2001.

Invited Talks

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| Georgia Institute of Technology (Host: Prof. David Bader) Title: “Parallel Computing – A Theoretical Perspective” | March 17, 2011 |
| Karlsruhe Institute of Technology (Host: Prof. Dr. Peter Sanders) Title: “Parallel Computing – A Theoretical Perspective” | December 21, 2010 |
| Goethe University Frankfurt (Host: Prof. Dr. Ulrich Meyer) Title: “Parallel Computing – A Theoretical Perspective” | December 20, 2010 |
| University of California, Irvine (Host: Prof. Michael Goodrich) Title: “Geometric algorithms for private-cache chip multiprocessors” | April 30, 2010 |
| Cambridge University (Host: Prof. Simon Moore) Title: “Parallel external memory model for multicore architectures” | April 22, 2009 |
| Dalhousie University (Host: Prof. Norbert Zeh) Title: “Parallel external memory model for multicore architectures” | October 16, 2008 |

Leadership and Professional Service

Reviewer for Journal of the ACM (JACM), Algorithmica, International Journal of Computational Geometry and Applications (IJCGA), IEEE Transactions on Parallel and Distributed Systems (TPDS), Parallel Computing, Computational Geometry: Theory and Applications (CGTA), ACM-SIAM Symposium on Discrete Algorithms (SODA), ACM SIGSPATIAL International Conference on Advances in Geographic Information Systems (ACM SIGSPATIAL GIS), Symposium on Experimental Algorithms (SEA), Latin American Theoretical Informatics Symposium (LATIN)

Council member of the Association of Graduate Students, *Univ. of California, Irvine* 2008 – 2009

REFERENCES

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