

Nodari Sitchinava

CONTACT INFORMATION	Department of Computer Science School of Information & Computer Sciences University of California, Irvine CA 92697	<i>Phone:</i> (650) 504-2608 <i>E-mail:</i> nodari@ics.uci.edu <i>Web:</i> http://www.ics.uci.edu/~nodari/
RESEARCH INTERESTS	Algorithms for multi-core architectures, parallel external memory and cache-oblivious algorithms, geometric and graph algorithms	
EDUCATION	University of California, Irvine <ul style="list-style-type: none">◇ Ph.D. Candidate in Computer Science, expected June 2009 Thesis: “Parallel external memory model and algorithms for multicore architectures” Advisor: Michael T. Goodrich Massachusetts Institute of Technology <ul style="list-style-type: none">◇ M.Eng. in Electrical Engineering and Computer Science, September 2003 Thesis: “Dynamic scan chains – a novel architecture to lower the cost of VLSI test” Advisors: Rohit Kapur and Daniel A. Spielman◇ S.B. in Electrical Engineering and Computer Science, June 2002	
RESEARCH EXPERIENCE	University of California, Irvine <i>Graduate Student Researcher</i> Advisor: Prof. Michael T. Goodrich Thesis research on developing a parallel computational model in the presence of private/shared memory hierarchy for multicore microprocessors. Design and analysis of algorithms in the new model.	Irvine, CA Sept. 2005 – present
	Dalhousie University <i>Visting Student Researcher</i> Research on parallel algorithms in computational geometry in the presence of private caches.	Halifax, NS, CANADA Fall 2008
	MADALGO, University of Aarhus <i>Visting Student Researcher</i> Research on parallel tree and graph algorithms in the presence of private caches.	Aarhus, DENMARK Summer 2008
	<i>Visting Student Researcher</i> Initial research on the fundamental parallel algorithms (such as sorting, selection and multiway partitioning) in the presence of private caches.	Summer 2007
	University of California, Irvine <i>Graduate Student Researcher</i> Research on reducing the complexity of cryptographically secure pseudo-random generators (PRGs). Supervisor: Prof. Stanislaw Jarecki	Irvine, CA Summer 2005
	Synopsys, Inc. <i>Research & Development Engineer in VLSI Test R&D Group</i> Investigation and development of a new technology to lower the cost of VLSI test via fault coverage estimation early in the design cycle.	Mountain View, CA Sept. 2003 – Sept. 2004
	<i>Research Internship in VLSI Test R&D Group</i> Research in the area of low cost VLSI test. Researched and analyzed Dynamic Scan architecture, as well as an extension to the Illinois Scan architecture incorporating the Dynamic Scan concepts.	Summers 2000, 2001; June – Dec. 2002

TEACHING
EXPERIENCE

Invited Lecturer, MADALGO, University of Aarhus Summer 2008
Prepared and presented a set of lectures on the topic “Parallel Algorithms for Private Caches” as a co-lecturer at the MADALGO Summer School on Cache-Oblivious Algorithms. Other lecturers included Professors Gerth Brodal, Erik Demaine and Norbert Zeh. Attended by 60 faculty, graduate students and post-docs.

Invited Lecturer, UC Irvine Spring 2008
Prepared and presented a lecture on cache-oblivious data structures in Prof. David Eppstein’s graduate course ICS 261 “Data Structures”.

Teaching Assistant, UC Irvine Summer 2007
Assisted Prof. Daniel Hirschberg in the course ICS 161 “Design and Analysis of Algorithms”. Prepared and taught sections reinforcing the material presented in lectures; graded homeworks and exams.

Teaching Assistant, UC Irvine Spring 2005
Assisted Prof. David Eppstein with course ICS 161 “Design and Analysis of Algorithms”. Prepared and taught sections reinforcing the material presented in lectures; prepared and presented a lecture on NP-completeness; graded exams.

Teaching Assistant, UC Irvine Winter 2005
Assisted Prof. Sandy Irani with course ICS H23 “Honors Introduction to Computer Science III”. Conducted and graded labs; prepared and presented a lecture on code testing and Java assertions.

Teaching Assistant, Massachusetts Institute of Technology Spring 2003
Assisted Prof. Ronald Rivest with course 6.045 “Automata, Computability and Complexity”. Prepared and taught sections reinforcing the material presented in lectures; graded exams.

AWARDS AND
ACHIEVEMENTS

- ◇ GSR/TA Fellowship, University of California, Irvine (Sept. 2004 – June 2005)
- ◇ Freedom Support Act Future Leaders Exchange (FSA/FLEX) program scholarship (1997 – 98)
- ◇ First and third place medals in regional math and physics competitions, Broken Bow, OK (1998)
- ◇ Finalist of The National Olympiad in Informatics, Tbilisi, Republic of Georgia (1996, 1997)

PUBLICATIONS

1. Refereed Conference Publications

- ◇ L. Arge, M.T. Goodrich, M. Nelson, N. Sitchinava. Fundamental parallel algorithms for private-cache chip multiprocessors. In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 197-206, 2008.
- ◇ D. Eppstein, M.T. Goodrich, N. Sitchinava. Guard placement for efficient point-in-polygon proofs. In *Proceedings of the 23rd Annual ACM Symposium on Computational Geometry (SoCG)*, pages 27-36, 2007.
- ◇ N. Sitchinava, S. Samaranayake, R. Kapur, E. Gizdarski, F. Neuveux, T.W. Williams. Changing scan enable during shift. In *Proceedings of the 22nd IEEE VLSI Test Symposium (VTS)*, pages 73-78, 2004.
- ◇ S. Samaranayake, E. Gizdarski, N. Sitchinava, F. Neuveux, R. Kapur, T.W. Williams. A reconfigurable shared scan-in architecture. In *Proceedings of the 21st IEEE VLSI Test Symposium (VTS)*, pages 9-14, 2003.

2. Journal Papers

- ◇ S. Samaranayake, N. Sitchinava, R. Kapur, M. Amin, T.W. Williams. Dynamic Scan: driving down the cost of test. *IEEE Computer* 35(10): 63-68 (2002).

3. Patents

- ◇ R. Kapur, N. Sitchinava, S. Samaranayake, E. Gizdarski, F. Neuveux, S. Duggirala, T.W. Williams. Dynamically reconfigurable shared scan-in test architecture. US Patent 7,418,640. 26 August 2008.

4. Papers in Preparation

- ◇ N. Sitchinava, N. Zeh. Parallel external memory computational geometry. In preparation, 2009.
- ◇ L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory graph algorithms. Under submission, 2009.
- ◇ D. Eppstein, M.T. Goodrich, N. Sitchinava. Foundational algorithms for distributed robot swarms. Manuscript, 2007.

PRESENTATIONS

1. Invited Talks

- ◇ Dalhousie University (Host: Norbert Zeh) Oct. 16, 2008
Title: “Parallel external memory model for multicore architectures”

2. Workshop Presentations and Posters

- ◇ N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams. Dynamically reconfigurable shared scan-in architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2004.
- ◇ N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams, D. Spielman. A segment identification algorithms for a dynamic scan architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2003.
- ◇ N. Sitchinava, S. Samaranayake, R. Kapur, M. Amin, T.W. Williams. DFT – ATE solution to lower the cost of test. *IEEE Workshop on Test Resource Partitioning*, 2001.

SCIENTIFIC SERVICE

- ◇ Journal referee: Journal of the ACM (JACM), International Journal of Computational Geometry and Applications (IJCGA), Parallel Computing

PERSONAL INTERESTS

- ◇ MIT varsity crew (1999 – 2003)
- ◇ Soccer, snowboarding, surfing, aikido