PARTHA BISWAS

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Interests

Compilers and Architectures for Embedded Systems, Application-Specific Processors.

Work Experience

University of California, Irvine, CA, USA
2000-Present — Graduate Student Researcher
Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland
Aug-Oct'2005 — Intern
Sep-Dec'2003 — Intern
STMicroelectronics, San Diego, CA, USA
Jun-Sep'2002 — Intern
Cadence Design Systems, Noida, India
1999-2000 — Member of Technical Staff
1998-1999 — Software Engineer

Awards

- Nominated for Best Paper in *DATE*, 2006.
- Nominated for Best Paper in *VLSI Design*, 2006.
- Nominated for Best Paper in *WASP*, 2004.
- Selected as a Best Paper in *CASES*, 2003 for publication in the special section of IEEE Transactions on Computers, 2005.
- Tuition Fellowship (2000-Present), University of California, Irvine, CA, USA.
- SPOT Award (Nov'1999), Cadence Design Systems, Noida, India.
- GEM Award (Apr'2000), Cadence Design Systems, Noida, India.

Education

Ph.D. in Embedded Systems, expected December 2005
Thesis: Acceleration of Computation beyond Memory Barriers in Extensible Processors
Advisor: Prof. Nikil D. Dutt
University of California, Irvine, CA, USA

M.S. in Computer System Design, awarded May 2002
University of California, Irvine, CA, USA

B.Tech. in Computer Science and Engineering, awarded June 1998
Indian Institute of Technology, Kharagpur, India

Selected Publications

- **Application-Specific Processors**

  P. Biswas, L. Pozzi, P. Ienne, and N. Dutt, *Automatic Identification of Application-Specific Functional Units with Architecturally Visible Storage*. To Appear in Proceedings of **Design, Automation, and Test in Europe (DATE)**, 2006.

  P. Biswas, S. Banerjee, N. Dutt, L. Pozzi, and P. Ienne, *ISEGEN: An Iterative-Improvement-based ISE Generation Technique for Fast Customization of Processors*. Submitted to **IEEE Transactions on VLSI**, 2005.

  P. Biswas, S. Banerjee, N. Dutt, P. Ienne, and L. Pozzi, *Performance and Energy Benefits of Instruction Set Extensions in an FPGA Soft Core*. In Proceedings of **VLSI Design**, 2006.

  P. Biswas, S. Banerjee, N. Dutt, L. Pozzi, and P. Ienne, *ISEGEN: Generation of High-Quality Instruction Set Extensions by Iterative Improvement*. In Proceedings of **Design, Automation, and Test in Europe (DATE)**, 2005.

  P. Biswas, S. Banerjee, N. Dutt, L. Pozzi, and P. Ienne, *Fast Automated Generation of High-Quality Instruction Set Extensions for Processor Customization*. In Proceedings of **Workshop on Application Specific Processors (WASP)**, 2004.

  P. Biswas, V. Choudhary, K. Atasu, L. Pozzi, P. Ienne, and N. Dutt, *Introduction of Local Memory Elements in Instruction Set Extensions*. In Proceedings of **Design Automation Conference (DAC)**, 2004.

- **Code Size Reduction**

  P. Biswas, and N. Dutt, *Code Size Reduction in Heterogeneous-Connectivity-based DSPs using Instruction Set Extensions*. Appeared in **IEEE Transactions on Computers (TC)**, 2005.

  A. Shrivastava, P. Biswas, A. Halambi, N. Dutt, and A. Nicolau, *A Compilation Framework for Code Size Reduction using Reduced Bit-width ISAs*. To appear in **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, 2005.

  P. Biswas, and N. Dutt, *Reducing Code Size for Heterogeneous-Connectivity-Based VLIW DSPs through Synthesis of Instruction Set Extensions*. In Proceedings of **International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)**, 2003.

  A. Halambi, A. Shrivastava, P. Biswas, N. Dutt, and A. Nicolau, *An Efficient Compiler Technique for Code Size Reduction Reduction using Reduced Bit-width ISAs*. In Proceedings of **Design, Automation, and Test in Europe (DATE)**, 2002.

  P. Biswas, and N. Dutt, A. Halambi, A. Shrivastava, P. Biswas, N. Dutt, and A. Nicolau, *A Design Space Exploration Framework for Reduced Bit-width Instruction Set Architecture (rISA) Design*. In Proceedings of **International Symposium on System Synthesis (ISSS)**, 2002.

Projects Undertaken

UCI **2000-2005** **(Advisor: Prof. N. D. Dutt)**

PhD Thesis: Acceleration of Computation beyond Memory Barriers in Extensible Processors

Performance of applications can be boosted by extending the target processor architecture with Application-specific Functional Units (AFUs). These AFUs accelerate the data flow in the critical segments of the applications by executing Instruction Set Extensions (ISEs). Our problem centers around how to automatically generate such ISEs under microarchitectural constraints. During the execution of an application, data gets transferred through different storage resources, for example, from main memory to cache and finally to register file. The AFU-based approach goes beyond the register file boundaries and accelerates the application. Our goal is to take this approach to its limit by bringing all possible sources of data directly inside the AFU and thus obtain the dual benefit of speedup and energy reduction.

ISEGEN: Generation of High-quality Instruction Set Extensions

A key step toward processor customization is generation of Instruction Set Extensions (ISEs). We presented an automatic technique for generation of ISEs, which was based on the basic principles of Kernighan-Lin min-cut heuristic. Our goal was to match the solution quality of experienced designers [**WASP04, DATE05**].

Evaluation of Instruction Set Extensions on a Real Platform

We targeted Xilinx Virtex II board and customized Microblaze soft-processor to study the effect of Instruction Set Extensions on performance, code size, power and energy [**VLSI-DESIGN06**].

Reducing Code Size for Heterogeneous-Connectivity-based VLIW-DSP Architectures

Modern VLIW-DSP architectures exhibit heterogeneous connections between functional units and register files for speeding up special tasks. We generated complex Instruction Set Extensions that effectively exploit such heterogeneous connections and result in code size reduction [**CASES03**].

Design Space Exploration for reduced bit-width Instruction Set Architecture (rISA)

We developed compiler optimizations to generate high-density code for architectures having a dual instruction set like ARM Thumb. We also performed exploration of rISA design space and came up with a rISA Instruction Set for a given application [**ISSS02, DATE02**].

Retargetable Assembly Generation in EXPRESSION

We added a pass to generate assembly code targeting a given architectural specification in EXPRESSION.

EPFL **Sep-Dec'2003** **(Mentor: Prof. P. Ienne)**

Introduction of Local Memory Elements in Instruction Set Extensions

Memory operations in general act as barriers for generation of Instruction Set Extensions (ISEs). However, we considered inclusion of local memory elements in the form of state registers and read-only memories in ISEs to increase their scope and thus gained both increase in performance and energy reduction [**DAC04**].

EPFL **Aug-Oct'2005** **(Mentor: Prof. P. Ienne)**
Automatic Identification of Instruction Set Extensions with Architecturally Visible Storage
We proposed the first ISE identification technique that can automatically identify state-holding ISEs comprehensively. The resulting ISEs eliminated a large portion of memory traffic and thus achieved further gain in performance as well as energy reduction [**DATE06**].

STMicroelectronics **Jun-Sep'2002** **(Mentor: A. Driker)**
Front-end of ST122 Assembly Optmizer for Coprocessor Extensions
In this small project, I wrote a front-end that reads ST122 assembly code and generates control flow and data flow graphs for a given application.

Cadence Design Systems **1998-2000** **(Manager: Dr. N. K. Jain)**
Development/Enhancement of some well-known Cadence tools
The tools were Analog Artist Netlisters, Preview LEF/DEF translaters, EDIF 300 translators, and CDLOUT.

IIT Kharagpur **1997-1998** **(Advisor: Prof. P. P. Das)**
Bachelor's Thesis: Design, simulation and synthesis of a hardware for performing fractal image compression

Other Activities

- Served as a Teaching Assistant for *ICS-151: Digital Logic Design* five times.
- Steered a public release of EXPRESSION, a retargetable compiler-simulator toolkit.
- Reviewed papers that appeared in journals, conferences and workshops such as *Journal of Systems and Software*, *DATE*, *DAC*, *CASES*, *CODES-ISSS*, *ICCAD*, *ISLPED*, *WASP*, *ESTIMedia*, etc.

References

- Prof. Nikil Dutt, UCI, `dutt@cecs.uci.edu`
- Prof. Paolo Ienne, EPFL, `paolo.ienne@epfl.ch`
- Prof. Laura Pozzi, University of Lugano, `laura.pozzi@unisi.ch`
- Prof. Alex Nicolau, UCI, `nicolau@cecs.uci.edu`
- Prof. Tony Givargis, UCI, `givargis@cecs.uci.edu`
- Alex Driker, STMicroelectronics, `alexander.driker@st.com`

Homepage

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