

From the EIC

A “powerful” issue!

■ **THE CLASSICAL SCALING FACTOR** of 0.7 on linear dimensions has defined the progression of process technology nodes. Silicon area shrinks by 0.49 and contains 0.7 times the capacitance, yielding a capacitance per unit area of 1.43 (a factor that roughly defines the increase in operating frequency per process generation). If supply voltage also decreased by 30%, power per unit area would remain roughly constant. Unfortunately, supply voltage scaling is slow, causing increases in power density. These increases have become increasingly important for scaling below 0.25 micron because of issues such as leakage, increased die size, and high-performance circuit designs. In fact, subthreshold leakage increases by 5× with each new process generation below 0.25 micron. Accordingly to Intel’s Shekhar Borkar, this leakage alone could account for almost 100 W in a 30-million-transistor chip at the 45-nm process node.

Power presents challenges at all design levels. Both architectural and circuit-level efficiencies for power continue to drop. Leading-edge processor architectures provide 1.4× to 1.7× performance growth for about a 2.5× increase in power. Even worse, most power-saving techniques reduce average power but increase power variability. Drops in V_{DD} make chips more vulnerable to this variability, including the effects of noise and dI/dt . Because higher-leakage parts are also higher-performance (and, therefore, higher-priced) parts, bin splits for leakage impact process yields.

Power now defines a constraint and a challenge for design, test, and manufacturing—one that smart engineers look forward to tackling! Power grids, at the forefront of this challenge, must deliver increasing currents (at lower voltages) while still maintaining decent noise margins. Design decisions at all levels have implications on the power distribution network and must take this into account. Guest Editors Sani Nassif and Soha Hassoun have selected an excellent set of articles that

provide solutions to these pressing problems.

This issue also includes a special section on infrastructure IP—a continuation of a theme from the May-June 2002 issue. These articles address BIST and self-repair techniques for digital filters, flexible SoC-level testing using customized test generation, test and repair for embedded memory, and IP blocks for board-level systems.

Finally, a special DAC Watch section commemorates the 40th Design Automation Conference. DAC has consistently been at the center of a thriving community of researchers and practitioners in electronic design automation. DAC Watch includes an overview of this year’s DAC technical program by Luciano Lavagno and Limor Fix (the technical program cochairs); a perspective by Alberto Sangiovanni-Vincentelli on DAC’s 40th birthday; and interviews with DAC personalities, including founder Pat Pistilli. The *D&T* editorial board and I thank the DAC executive committee and Chair Ian Getreu for making this special section possible. We also thank all the program and general chairs of previous DACs for their comments on DAC highlights and challenges. Richard Newton, in a special sidebar, succinctly captures these challenges and how DAC has responded to them to create new growth opportunities.

We are also happy to coorganize an interview with ARM founder Sir Robin Saxby, a panel discussion on technology developments in deep-submicron technology, and a roundtable discussion at DAC. We hope to see you there. Enjoy this issue!



Rajesh Gupta
Editor in Chief
IEEE Design & Test of Computers

