

From the EIC

At-speed testing: A shared red brick between design and test



■ **LAST ISSUE**, I talked about the problems-of-the-large in design and verification tasks for system chips. Beyond size, the accelerating upward trend in operating frequencies for chips used in almost all application domains has tremendous implications for both chip design and manufacturing. The problem arises not only from the increasing scale of tasks performed on-chip but also the process complexity—more-complex fabrication steps that must deal with many copper and aluminum wiring levels; various k dielectrics; and multiple threshold devices. From a manufacturing-test point of view, these changes alter the nature of the defects and immensely complicate the task of timing analysis and path selection for testing and for grading the finished chips. The cost of test equipment skyrockets at very high-frequency chip-board interfaces. Because interfaces must handle high-speed testing, part of the testing equipment invariably finds itself inside the chip—that is, smart BIST solutions are part of the design.

At-speed testing is crucial for reducing test time and in capturing frequency-dependent defect mechanisms that arise from process complexities. Such testing defines the interface where problems of the small (such as process variability or new defect mechanisms) meet problems of the large (such as increasing test data volume and test time). Indeed, the *International Technology Roadmap for Semiconductors* (ITRS) treats the ATE challenges as a *red brick*, that is, “a technology requirement for which no known solution exists.” It is also a *shared red brick*, shared between the ATE and design technology groups. The common challenge is to ensure that the test interfaces remain viable in terms of cost and robust against process variability, according to Andrew Kahng of the University of California, San Diego, who coined the phrase in his introductory RoadAhead column last year. Guest editors Ken Butler, Tim Cheng, and L-C. Wang have put together an excellent special issue on this topic with articles ranging from structural test for new process tech-

nologies to AC scan and statistical post-processing.

This issue also contains a special section on breaking test interface bottlenecks, the theme of this year’s International Test Conference. ITC is the primary event covering the testing of devices, boards, and systems. Under the leadership of the Test Technology Technical Council, *D&T* is proud to be part of a special relationship with ITC. Every year, *D&T* publishes a special section on the ITC theme for distribution at ITC.

So as part of this ITC Watch, Rob Aitken and Gordon Roberts put together a special section on test interface issues. It nicely supplements the subject of at-speed testing and binning in this issue, expanding the test boundary to include wafer/package test to reduce test time.

As another part of this special section, Ben Bennetts discusses efforts to enhance ITC’s offerings in the area of board test. He surveys the ITC sessions, lecture series, and panels that have come about because of this special emphasis.

I hope you enjoy this issue!

A handwritten signature in black ink that reads "Rajesh Gupta". The signature is written in a cursive, flowing style.

Rajesh Gupta, Editor in Chief

A proposal for EDAtch

In the November–December issue, Alberto Sangiovanni-Vincentelli (University of California, Berkeley) will propose EDAtch—a government-industry-university cooperative that would take on the substantial design and test challenges. The value of such cooperation is supported by commentaries from Bill Spencer, chair emeritus of Sematech; and Ken Flamm, Dean Rusk Chair in International Affairs, LBJ School of Public Affairs, University of Texas, Austin.