

The changing face of IC design and its industry



■ **SEMICONDUCTOR IC DESIGN** and manufacturing are facing a structural shift in the industry. As manufacturing migrates offshore to low-labor-cost markets, it is leaving behind IC design houses to compete in a marketplace with “commodity” semiconductor processes and design tools. The challenge for the new IC designer is to deliver verifiable silicon designs ready for manufacture in rapidly shrinking time windows, a process that makes it necessary to reuse chip designs. In this issue, *Design & Test* examines the impact of these challenges on one of the most basic tenets of IC design: clocking circuits and methodologies.

Synchronous design has thus far been the mainstay of chip designs and design tools for a very good reason: A single clock reference simplifies synchronization, timing analysis, and circuit design. However, clocks are imperfect, and becoming more so with each new process generation. Skew among clock signals eats into valuable clock period. The clocking tree is a major consumer of dynamic power and, worst of all, it obstructs design reuse by placing strict uniformity requirements on the clock distribution and storage elements used across different IP blocks.

It is, therefore, tempting to think of what a chip design would be like without clocks. Researchers have explored such a world in some depth, in the form of asynchronous circuits and methodologies. These special cases of clockless circuits have strong requirements on delay insensitivity and designers can learn a lot from such circuits in designing future SoCs with islands of clocked and clockless IP blocks. Because of the subtleties inherent in asynchronous-circuit designs, tool support is critical to ensure design correctness. Guest Editors Yong-Bin Kim and Fabrizio Lombardi have pulled together an excellent special issue covering both the advances in the practice of clockless circuit design as well as design methodology and tools.

This issue also contains a special section addressing challenges for the changing semiconductor industry in

ensuring that it continues to drive economic growth and be the major employer of engineering talent, arguably a difficult assignment given that semiconductors account for over 6% of the national *manufacturing* GDP. In an in-depth interview with *D&T*, Michael Hackworth, Cirrus Logic’s chairman of the board, examines the shifting landscape in semiconductor industry and its lessons.

Earlier this year, Alberto Sangiovanni-Vincentelli of the University of California, Berkeley, delivered a fascinating review of the EDA industry’s evolution. Embedded in it were strong lessons for this industry’s future. He outlines his proposal for a Sematech-style initiative, called EDAtch. Sematech is widely credited with having nurtured competitiveness in semiconductor industry by—among other things—directly supporting research and development activities in its supplier industry, semiconductor equipment manufacturing.

This special section features commentaries by William Spencer, Sematech’s chairman emeritus; Kenneth Flamm, an economic-policy expert at the University of Texas, Austin; Ray Bingham, CEO of Cadence Design Systems; and Fred Shlapak, Executive Vice President of Motorola. Taken together, these make a compelling case for a concerted government-industry-academia initiative to support the emerging semiconductor systems industry. Such support would be a catalyst in building an even more powerful engine of economic growth than semiconductor manufacturing of previous decades. We are glad to be at the forefront of this important debate. We invite you to join the discussion by writing your opinions to rgupta@ucsd.edu.

A handwritten signature in cursive script that reads "Rajesh Gupta".

Rajesh Gupta
Editor in Chief
IEEE Design & Test of Computers