

# Driving Research in System-Chip Design Technology

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**W**e revere Moore's law. Depending upon the occasion, it can seem like a natural phenomenon, a commandment, or a mantra to a future of ubiquitous riches.

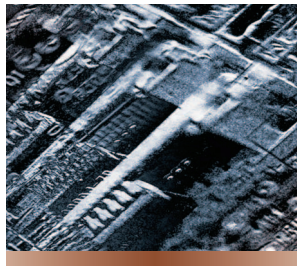
Indeed, semiconductor advances over the past three decades have been tremendous. They have engendered a new economy of continuously falling electronics prices and increasing systems capabilities—all driven fundamentally by increased integrated circuit yields.

And we solemnly hope that these trends continue.

## PROCESS PLANNING

To ensure that they do, the semiconductor industry invests heavily in planning for future processes through its privately funded Sematech consortium. Launched in 1988 with US government help, Sematech helped define technology policy and return semiconductor industry leadership to the US. Since 1996, the consortium's funding has come entirely from industry, which—to a large extent—drives Moore's law into practice.

Indeed, the now International Sematech consortium analyzes process technology needs continually in a living document, the *International Technology Roadmap for Semiconductors* (<http://public.itrs.net/>). In substantial detail, the ITRS maps where chip designers can expect semiconductor



**Process technology advances must be matched by investments in design technology for application-oriented system chips.**

process capabilities to be a few years hence. This in turn establishes the baseline for managers everywhere to set their own process technology goals and for semiconductor equipment makers to plan accordingly.

Small wonder that in the nine-plus years since this exercise began, the roadmap predictions have actually fallen short of real process maturity. For example, we are currently producing chips using 130-nm process technologies, which the ITRS originally predicted would come online no sooner than 2007—if the constituent process developments went as planned.

On the other hand, it seems that problems in manufacturing yield and unclear advantages in the application space are delaying the 90-nm technology node.

## 100-NM INFLECTION POINT

A 100-nm process technology node defines an inflection point for both system designers and process engineers. For system designers, it brings 100-million-transistor chips within reach. At

the same time, it opens new process challenges. In fact, ITRS experts have identified a number of “brick walls”—technical problems for which no known solutions exist—that the industry must overcome to continue its progress beyond 100-nm technology nodes.

For the first time, we face the need for new materials, new process technology, and new design methods. According to a May 2001 study for the Semiconductor Research Corporation, meeting these challenges will require an additional \$400 million of developmental investment—roughly half

the current worldwide R&D spending in microelectronics.

Foundries or fabs—whether independent or part of a semiconductor design house, the so-called integrated device manufacturers (IDM)—are at the forefront of this manufacturing challenge and specializing as independent businesses themselves. To stay competitive, most independent foundries now routinely sport process technology roadmaps that exceed those of the IDM foundries.

However, owning and running a foundry is a challenging business proposition. A fab costs \$4 billion to build today, and it must derive \$6 billion per year in revenue to be sustainable. Of the dozen or so foundries in the world, only a handful actually meet this criterion.

With current fab utilization running anywhere from 60 to 80 percent, the spare capacity in rapidly depreciating equipment further challenges fab sustainability over the long term, forcing semiconductor manufacturing to low-cost labor markets.

### SYSTEM CHIPS

Yet there is a silver lining. The \$138 billion semiconductor industry is rapidly coming unbundled from a general-purpose to a segmented IC market for specialized applications, such as entertainment, networking, communications, consumer electronics, graphics, gaming, and appliances. This segmentation is effectively bringing better products to market sooner, creating rapid product update cycles and driving the much larger electronics industry.

The new chips—often called *system chips* because they contain full systems—are highly application-specific, with short market and architectural life cycles. In these systems, content increasingly determines computational processing, thus making embedded software an important part of system-chip design. Connection—or bandwidth delivery—is often more important than computational efficiency.

Designers must streamline these system architectures to support scalability and software adaptability. Semiconductor intellectual property is an important part of the competitive advantage, but it must be made viable through ownership of the architectural platforms and value-added software.

The part of the semiconductor industry that serves this need has been growing fast. The top 10 “fabless” design houses increased in revenue by 19 percent in 2002, compared to a 1.2 percent overall growth rate for the semiconductor industry. These design houses now constitute 15 percent of the worldwide semiconductor market, and—if we believe their expressed goals—could be half the total semiconductor market by 2010.

Even now, the fabless industry, which is almost as young as the foundries it uses, exceeds the foundry industry in revenues. By all measures, this industry is not only growing but could be the chief recruiter of future engineering talent in this country. However, it cannot sustain this growth unless we address fundamental challenges in design technology and cost of design now.

### BEYOND PROCESS TO DESIGN

Designing and verifying system chips demands a changing skill set that brings an IC designer closer to a domain expert. A chip designer in a networking industry must also be conversant with network engineering fundamentals. The same goes for wireless or gaming applications.

**Intellectual property is critical to the new semiconductor industry's success.**

The design challenges for system chips go far beyond the process technology headaches. With the design and test backend delegated to standard flows and tools from outside vendors, the design focus is necessarily at the system level. In addition, as system companies shift R&D costs to their suppliers in the disaggregated economy model, system-level design becomes a critical interface between system and implementation companies.

The challenges of the embedded software and development environments directly affect the system design industry. Intellectual property is no longer a productivity issue; it is critical to the new semiconductor industry, which will succeed only if it can guarantee IP viability.

### DESIGN TECHNOLOGY

Similar to the process brick walls, the design technology for system chips faces formidable challenges:

- traditional computer *architecture design* is no longer sufficient or even helpful, and system-chip architects need new architectural design principles to guide their work;
- the *programming context*—that is, what happens in hardware or software, what the compiler or the runtime system does—is due for an overhaul; and
- the *contract* between the application and system software must

change radically as system chips demand new operating-environment capabilities, such as power and location awareness, reactive behavior, and stability with tight control software loops.

If indeed we are capable of producing chips with millions and millions of gates, we are nevertheless incapable of bringing error-free designs to market quickly. The design of complex systems is becoming a bottleneck more serious than mastering the process technology. This has a direct adverse impact on how quickly and economically we can bring new capabilities from advancing silicon into military and civilian systems.

### RESEARCH DISCONNECT

The portfolios of our federal research sponsors do not reflect these changes. Indeed, referring to a famous quote by AMD's Jerry Sanders, the policy makers' mindset is “real men (semiconductor houses) have fabs.”

To be sure, the industry's immediate manufacturing needs are the primary driving force for material and process technology investments, much of them by industry consortia. However, microelectronic advances are intertwined: We must match investments in process technology with investments in applications, system software, and system-chip design technology.

Researchers must take the lead in building prototypes. Innovation will depend on the tools we have and our ability to build and test prototypes. This capability has been slowly moving away from most universities in the US for a variety of reasons—among them, a shifting research agenda by US government agencies that drive innovations in systems capabilities, such as the Defense Advanced Research Projects Agency and the scientific agenda at the National Science Foundation.

A disconnect exists between the investments being made to solve large-scale information technology problems (as exemplified by the successful Infor-

mation Technology Research program at NSF) and those to address the design and process technology needs that lie at the heart of our IT capabilities.

Our ability to architect, design, program, and validate future generations of system chips will be crucial to our capabilities in a variety of IT and military command and control capabilities. As the gap between “box makers” and semiconductor designers continues to widen, commercial and military design technology leaves an increasing amount of performance on the table. For instance, typical ASIC flows support maximum 500-MHz parts on processes that can easily handle more than 2-GHz parts. This gap continues to widen at an alarming rate for the coming sub-100-nm processes, thus rapidly moving semiconductor technology advances out of the reach of specialized (low volume) box makers.

#### ENTERING A NEW ERA

We are entering a new era in IC design in which the ability to design and verify is perhaps more crucial than having access to the most advanced

process. We need strong implementation capabilities, yet the shifting emphasis in research from industrial laboratories to universities hits precisely these capabilities.

Given the sophistication of the design tools, some argue that electronic design automation companies should assume responsibility for driving the agenda in design innovation. However, the EDA industry today is focusing on ASIC-like design flows, where the market is largest.

The market for more advanced design methods and tools is not large enough to reward the investment made to advance the state of the art. Traditional system and technology companies with a strong research component such as IBM and Bell Labs are either no longer engaging in EDA research or looking aggressively to outsource this capability.

Going forward, we can only hope that, along with process advances, system-level design and validation issues will get the attention they need while we still have the high ground on IC implementation capabilities.

**W**e need a national agenda for research in system chips. The Sematech experiment shows that, given government leadership, the industry is quite capable of defining the research agenda and mobilizing the resources to build on its success. The challenge is to keep the economic implications of a continued Moore’s law from compromising our fabled future by feeding the spiraling costs of design. ■

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