



Deep-Submicron Challenges

■ This issue examines the challenges posed by deep-submicron technologies. Although deep-submicron microelectronic technologies enable greater degrees of semiconductor integration, such integration makes the design, verification, and test challenges more difficult. Designers try to handle the design and verification complexity through models and methodologies to raise the abstraction level, but process and device challenges still take their toll on the overall design and test. Consequently, microelectronic circuit design and test are often the first areas under assault by the effects of aggressive scaling in deep-submicron technologies. Such effects range from substrate coupling of noise and crosstalk to the use of very low threshold devices that make I_{DDQ} testing difficult.

The articles in this issue address these concerns. Two articles specifically examine circuit design with low supply voltages and the challenges such voltages cause in applying I_{DDQ} testing. Another article describes a promising technology from image processing that can potentially eliminate cumbersome manual work required to identify flawed wafer-scale regions.

Despite stellar increases in the scaling and integration of large-scale digital circuits, analog design continues to remain one of the least scalable areas of chip design. This issue includes an article on a procedure that uses a scalable model of the devices to enhance analog-circuit reuse. Finally, a nontheme article describes a model-based design methodology for embedded systems to improve hardware-software codesign and testing.

This issue also features the first installment of a new department: *The Road Ahead*, by our resident expert on the *International Technology*

Roadmap on Semiconductors, Andrew Kahng, who is from the University of California at San Diego. Andrew was one of the key contributors to the outlook on design technology in the recent *ITRS* revision. In this issue, Andrew discusses the notion of *red bricks*, a technological requirement for which the solution is not known. The *ITRS* looks 10 to 15 years into the microelectronic future with technologies that will push scaling to gate lengths as low as 0.009 micron. No wonder the *ITRS* is full of red bricks, when evolutionary improvements to several techniques simply will not work. Andrew proposes solutions that build a coordinated attack on microelectronic challenges.

I hope you enjoy this issue. The volunteers and staff of *IEEE Design & Test* constantly try to provide you with a balance of articles, from promising research to best practices, from technology solutions to design and test problems. As the microelectronic industry has grown, so has the level of sophistication and specialization in design, validation, and test tools. With this issue, I am pleased to welcome three new area editors who will help us keep up with upcoming technology challenges: Grant Martin from Cadence Labs, who will be the area editor for design reuse; Soha Hassoun from Tufts University, for system-on-a-chip design; and Sharad Malik from Princeton University, for embedded systems and software.

A handwritten signature in cursive script that reads "Rajesh Gupta".

Rajesh Gupta
Editor in Chief
IEEE Design & Test of Computers