

## From the EIC

# Enabling IP



For many years, the semiconductor intellectual-property (IP) market has presented tantalizing prospects for industry growth. *IEEE Design & Test's* first issue on the subject was in 1997, when we examined the evolving nature of IP cores. Since then, the IP component market has grown tremendously. Software IP such as drivers, protocol stacks, and signal-processing functions are beginning to constitute a separate, albeit still tiny, market segment. Semiconductor vendors had often given these IP blocks for free as a part of hardware IP.

However, the most exciting prospects today come from infrastructure IP blocks, which span the entire range of microelectronic system-on-a-chip design, manufacturing, and test. These include IP blocks for embedded test, yield optimization, debugging, and repair. According to Erach Desai in "The silicon infrastructure opportunity" (a sidebar in this issue's Guest Editor's Introduction), infrastructure IP is key to future growth and adoption of the IP-based system chips. Guest Editor Yervant Zorian has carefully put together this issue, with a collection of articles that critically examine the challenges, opportunities, and leading trends in infrastructure IP use for coming generations of system chips.

Among this issue's nontheme articles, an article by Andrew Caldwell and his coauthors examines another form of reuse, that of proven algorithms to solve fundamental CAD problems. Patrick Girard provides a survey of strategies that ensure low-power dissipation during test application. Alfredo Benso and his coauthors detail a case study of the combination of DFT strategies used in a multichip module design for multichannel data acquisition and signal processing.

This issue also features a roundtable on design and test education in Latin America. Finally, *The Road Ahead* column examines the role of variability in IC manufacturing and how designers are increasingly being called on to address this variability up front, perhaps even modifying the design optimization goals.

I am happy to introduce our latest addition to the editorial board, Fadi Kurdahi, from the University of California, Irvine. Beginning with this issue, Kurdahi joins us as an area editor for configurable computing. I would also like to thank Joe Damore for his past contributions as area editor for computer-aided engineering. We are fortunate to have Joe continue as our liaison to the IEEE Computer Society's Design Automation Technical Committee (DATC).

Special issues have been critical to *IEEE D&T's* success by focusing attention on timely subjects and providing state-of-the-art articles on research and practice. In the coming months, we have planned three more special issues: embedded-processor design, defect-oriented testing in the deep-submicron era, and platform-based design of SoCs. We depend on you, the readers, to provide timely articles. Furthermore, we select special-issue articles months in advance. We are currently choosing special-issue topics for 2003. If you have any suggestions, please drop me a line at [gupta@uci.edu](mailto:gupta@uci.edu).

I hope you enjoy this issue!

A handwritten signature in cursive script that reads "Rajesh Gupta".

**Rajesh Gupta**  
Editor in Chief  
*IEEE Design & Test of Computers*