

From the EIC

Full circle?



A recent report from International Business Strategies (*Analysis of the Relationship between EDA Expenditures and Competitive Positioning of IC Vendors*), a custom study for the EDA Consortium, correlates in-house design implementation expertise with market leadership position in later years, for several semiconductor companies. We have apparently come full circle in terms of what constitutes a competitive advantage for microelectronics design houses. In the past, the ability to design complex chips (with many hundreds of thousands of transistors) and successfully verify them against possible circuit and logic bugs was a capability confined only to design houses of a certain size and wherewithal—generally, integrated device manufacturers (IDMs). Only a few companies could afford the resources necessary to maintain expertise in the entire design process and build large-transistor-count or high-integration chips. But then college curricula caught up with industry, and industry devised design methodologies—including the division of labor between logic, circuit, and physical design—that led to the proliferation of design expertise.

Afterward, manufacturing—or, more precisely, access to advanced, in-house process technology—became the new competitive advantage. Despite the rise of foundries and EDA companies and the steady migration of ASIC chip design to system design houses, leading-edge chip designs still relied on access to leading-edge process technology. This technology still resided with the large IDMs.

More recently, however, the lag in process capabilities between foundries and IDMs has been shrinking. In fact, foundries like those owned by TSMC and UMC now sport technology roadmaps beyond 90 nm that rival IDM schedules. Now, everyone has access to advanced semiconductor processes. Once again, design implementation leadership will likely define the dominant platform for semiconductor IP.

Although we've apparently come full circle in terms of

a design-driven competitive advantage, the nature of design expertise has shifted. There is increasing architectural exploration in silicon, and steadily more attention paid to signal-integrity, low-power, and defect-tolerance issues in board-level design. Our November-December 2002 issue examined the silicon substrate as an architectural platform. Here, we consider the board-level challenges—specifically, those in test. Guest editors R.G. (Ben) Bennetts and Monica Lobetti-Bodoni have organized an excellent special issue on board-level test technologies.

As design proceeds to the system level, verification of implementation correctness becomes more challenging, because of both the increasing size of the task and the treatment of diverse system components. Miroslav Cupak, Francky Cathoor, and Hugo De Man discuss a strategy for system-level functional verification for multimedia applications. Chien-Nan Jimmy Liu, I-Ling Chen, and Jing-Yang Jou propose a technique for detecting specific source-level code fragments and their transformations that lets them improve verification by reducing the subsequent number of necessary functional test patterns. Nur Engin and Hans Kerkhoff discuss improvements to transient fault simulation in analog circuits using dc bias grouping. João Cardoso and Horácio Neto describe synthesis advances for FPGA platforms using Java bytecodes. Finally, in *The Last Byte*, Ken Parker takes on the tall claims of achieved test coverage often made by ATE equipment manufacturers.

I hope you enjoy this issue!

A handwritten signature in cursive script that reads "Rajesh Gupta".

Rajesh Gupta
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IEEE Design & Test of Computers