

The neglected community



■ **ADVANCES IN MICROELECTRONICS** design and test have traditionally been in step with process technology advances, but when it comes to R&D funding, design and test lag far behind. The magnitude of process technology challenges is increasing. Charles Nuese, in a study for the Semiconductor Research Corp. (SRC), grimly points out that overcoming process challenges beyond 100 nm will require an annual increase in microelectronics R&D funding of \$400 million—a roughly 50% increase in current worldwide R&D spending in microelectronics. Indeed, for the first time, we are faced with a situation in which new materials, new technology, and new design methods are needed.

While investment in materials and process technology—driven by immediate manufacturing needs—continues, R&D in design tools and methods lags behind. By unofficial counts, approximately 60% of SRC and SRC-leveraged R&D investments target process technology needs. The situation is even more skewed when you consider direct industry R&D expenditures by companies such as Intel. The funding situation gets much worse as we move to design and test at higher abstraction levels. However, the importance of research into system-level design and validation methods and tools cannot be overestimated. According to Justin Harlow of SRC, “into the foreseeable future, our ability to create meaningful, economically viable products is going to depend more heavily on our ability to design and verify them than on our ability to build them in far-nanometer technologies.”

Yet if you look at the portfolios of major research agencies, from the National Science Foundation (NSF) to the SRC, microelectronics system design appears to be on the fringe. By one account, of the \$254 million that the US

government spent on micro- or nanotechnology research in 2001, less than \$4 million went toward system-level design methods for microelectronic systems. This situation arises partly from the disconnect between the SRC and government funding programs. The latter are often driven by large-scale information technology (IT) needs, and fail to fully appreciate the role of microelectronics design and test underlying the advances in IT and telecommunications.

This issue focuses on an important development in system-level design methods—namely, platform-based designs—to address the growing complexity of on-chip system designs. Successful execution of design encapsulation as a platform is likely to provide the needed boost in design productivity and quality that the microelectronics industry needs to extend silicon’s reach to new applications and networks.

Reflecting the diversity of *D&T* readership, the nontheme articles in this issue address practical advances in oscillation-based testing, a design methodology for data path blocks, and techniques to minimize test escapes—undetected defects—in static voltage testing. In *The Road Ahead*, Andrew Kahng examines packaging’s significance in microelectronic-systems costs. Finally, in *The Last Byte*, Alberto Sangiovanni-Vincentelli makes a compelling case for expanding the concept of platform-based design as a general design approach for diverse embedded systems containing both software and hardware. I hope you enjoy this issue!

A handwritten signature in black ink that reads "Rajesh Gupta".

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