CS 151
Quiz 2

Name : ___________________ , ___________________
      (Last Name)                 (First Name)
Student ID : _______________
Signature : ________________

Instructions:

1. Please verify that your paper contains 6 pages including this cover.
2. Write down your Student-Id on the top of each page of this quiz.
3. This exam is closed book. No notes or other materials are permitted.
4. Total credits of this quiz are 50 points.
5. To receive credit you must show your work clearly.
6. No re-grades will be entertained if you use a pencil.
7. Calculators are NOT allowed.
Q1: [Latch analysis] [10 points]

Shown below is a NOR implementation of gated D-latch:

![NOR implementation of gated D-latch](image)

The timing diagrams of D and C are shown below. Show the timing diagram for Q and Q': (Assume that Q=0 at t0 and there is no gate delay) [10 points]

![Timing diagrams](image)
Q2: [FSM design] [15 points]

Design an FSM for a circuit which has a 2-bit input X and an output Y. The output Y becomes 1 if the cumulative sum of the numbers in sequence X multiple of 3. Otherwise Y is 0. [15 points]

For example:

X: 00 → 11 → 01 → 10 → 00 → 01 ...
Y: 1 → 1 → 0 → 0 → 1 → 0 ...


Q3: [Controller design] [25 points]

We want to design a complete sequential circuit for a sequence detector which can detect a sequence of 110 on its input X. When this sequence is detected the output Y will be equal to 1 for exactly one clock cycle:

The FSM is shown below:

a) Create the architecture for this FSM. [5 points]
b) Considering the state encoding shown below, draw the state table. [10 points]

A = 00, B = 01, C = 10, D = 11
c) Write the equations for the combinatorial logic. [10 points]