ICS 152, Problem Set 4

- Please show your work.
- Bottom line answers without proper explanation are worth **zero** points.

1. Text Problem 6.4

2. How could we modify the following code to make use of a delayed branch slot?

```
Loop: lw   $2, 100($3)
      addi $3, $3, 4
      beq  $3, $4, Loop
```

3. Text Problem 6.14

4. For each of these pieces of code, name the type of data hazard:

(a) *add $1, $2, $3*
sw $4, 0($1)

(b) *add $1, $2, $3*
sw $1, 0($4)

(c) *lw $1, 0($2)*
sw $1, 0($4)

(d) *lw $1, 0($2)*
sw $4, 0($1)

(e) *lw $1, 0($2)*
add $1, $1, $2

5. Suppose MIPS has a new instruction *subnz* (subtract non-zero) that has the same R-type format as a regular *sub* instruction, except that the destination register *rd* is updated only if the difference between the values of the *rs* and *rt* registers is non-zero.

(a) Give a short piece of code containing a data hazard involving a *subnz* instruction, when executed on the classic 5-stage MIPS pipeline without forwarding. Draw the pipeline diagram for your code, clearly indicating the location of stall(s).

(b) Can forwarding eliminate al l data-hazards involving *subnz* instructions? If so, write a hazard-detection condition for any situation where forwarding can resolve the data hazard. If not, write a stall-detection condition for any situation where a stall must occur to resolve the data hazard.

6. Text Problem 6.36

7. Text Problem 6.39