Bryan Donyanavard

34470 Via Verde
Dana Point, CA 92624
(661) 713 7479
bdonyana@uci.edu
www.ics.uci.edu/~bdonyana

Education

2013–present **Ph.D. in Computer Science**, *University of California, Irvine*, *GPA: 3.9*.
EGD: 2019 Awarded ICS Dean's Fellowship (4 Years of Full Financial Support)

2008–2010 **M.Sc. in Computer Engineering**, *University of California, Santa Barbara*, *GPA: 3.9*.

2004–2008 **B.Sc. in Computer Engineering**, *University of California, Santa Barbara*, *GPA: 3.3*.

Research & Work Experience

June. 2015 – present **Graduate Student Researcher**, Dutt Research Group, University of California, Irvine.
- Adaptive On-chip Memory Management in Future Many-core Systems
  - *Working on software solutions to simultaneously exploit the features of new memory technologies and application semantics during on-chip memory management in many-core systems*
- Adaptive and Autonomous Resource Management in Mobile Systems
  - *Providing policies in software for adaptive resource management of unpredictable workloads*
  - *Developing autonomous hierarchical supervisors to manage system goals in response to abrupt runtime changes*

July 2016 – Sept. 2016 **Software Engineering Intern**, Chrome OS, Google.
- Performed research in viability of non-volatile memory (NVM) main memory replacement for mobile SoCs. Proposed and evaluated large last-level cache controller policies for NVM main memory systems by extending the gem5 simulator.

June 2015 – Sept. 2015 **Software Engineering Intern**, Technical Infrastructure, Google.
- Performed platforms research in software management of multi-tiered main memory hierarchies. Evaluated the validity of incorporating non-uniform memory accesses in cloud applications by collecting and simulating memory traces from live workloads.

Jan. 2011 – Jan. 2013 **Software Developer**, SPARC Systems Group, Oracle.
- Member of platform development teams for SPARC Systems providing bootstrapping source code to initialize chip and system state. Developed firmware to manage various platform I/O peripherals. Platforms include SPARC Blade, Volume, and Enterprise.

Sept. 2010 – Jan. 2013 **Android Application Developer**, ProDIGIQ.
- Contracted to independently develop and release to market Android applications for multiple airports around the United States. Apps provide services including real time updates of flight time tables, local information regarding parking and rentals, and embedded forms to be electronically submitted.

July 2009 – Sept. 2010 **Engineer**, Special Technologies Laboratory, National Security Technologies.
- Designed mobile embedded sensor devices. Devices consist of RTOS running on a microcontroller managing peripheral sensor data as well as networked over multiple communication links. Developed device specific communication protocol. Integrated and implemented communication between devices and user interface software.

June 2007 – Sept. 2007 **Summer Intern**, Information Technology Solutions, Northrop Grumman.
- Coded, implemented, and presented a complete data storage management system from start to finish in conjunction with a Six Sigma project. Interface consisted of a web application form in Apache Struts framework using JavaServer Pages that performed queries and updates on an Oracle database. Contributed C code for matrix inversion in parallel across a cluster using Linux MPI library for modeling parasitic capacitive coupling.

Teaching & Mentoring Experience

Sept. 2017 - Dec. 2017 **Certificate in Teaching Excellence Program**, Division of Teaching Excellence and Innovation, University of California, Irvine.

- Trained and certified in designing lessons using evidence-based pedagogical principles, analyzing and assessing teaching practices, and effectively facilitating learning

Sept. 2017 - Dec. 2017 **Associate Training**, Center for the Integration of Research, Teaching and Learning, University of California, Irvine.

- Trained and certified in effective teaching and learning, and scholarly teaching that uses the CIRTL ideas to demonstrably improve learning of students

June 2017 – Jan. 2018 **Mentor**, International Summer Undergraduate Research Fellowship, University of California, Irvine.

- Proposed research projects for undergraduate interns
- Supervised four undergraduate students from Korean universities in completing proposed projects

Jan. 2014 – Jan. 2016 **Volunteer Tutor Lead**, Rocket Science Tutors, Santa Ana Unified School District.

- Lead mentor in after school program to encourage local students' involvement in STEM subjects
- Nominated for Engage UCI award for Excellence in Service

Summer 2010 **Graduate Student Mentor**, Apprentice Researchers Program, University of California, Santa Barbara.

- Spent 4 weeks as mentor aiding a high school student apprentice in completing an engineering research project

Instructor.

- Digital Logic Design, UC Irvine, Fall 2018

Teaching Assistant.

- Critical Writing (online)
- Digital Logic Design
- Critical Writing
- Intro to Programming
- Principles in System Design
- Computer Systems Architecture
- Programming in C++
- Introduction to Digital Systems
- Physics
- Digital Design Methodologies

Computer Skills

Programming Languages	C, C++, Java
Scripting	Python
Compilers	LLVM Compiler Infrastructure
HDLs	Verilog, VHDL
Architectural Simulators	gem5
EDA Tools	Mentor ModelSim, Cadence PSpice
FPGA Tools	Xilinx ISE
Miscellaneous	Git Version Control System, LaTeX

Research Interests

- Memory Management in Software and Architecture
- System Software for Heterogeneous Systems
- Computational Self-awareness
- Adaptive Resource Management for Mobile Systems

Publications

2019 Bryan Donyanavard, Armin Sadighi, Florian Maurer, Tiago Mück, Amir Rahmani, Andreas Herkersdorf, Nikil Dutt, **SOSA: Self-Optimizing Learning with Self-Adaptive Control for Hierarchical System-on-Chip Management**, *52nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*

2019 Eberle Rambo*, Bryan Donyanavard*, Minjun Seo*, Florian Maurer*, et al., **The Information Processing Factory: A Paradigm for Life Cycle Management of Dependable Systems**, *Embedded Systems Week Special Session (ESWEEK)*

2019 Biswadip Maity, Bryan Donyanavard, Nalini Venkatasubramanian, Nikil Dutt, **Workload Characterization for Memory Management in Emerging Embedded Platforms**, *The 6th International Embedded Systems Symposium (IESS)*

2018 Bryan Donyanavard, Amir Mahdi Hosseini Mozannah, Tiago Mück, Nikil Dutt, **Exploring Hybrid Memory Caches in Chip Multiprocessors**, *13th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*

2018 Amir Rahmani*, Bryan Donyanavard*, Tiago Mück*, Kasra Moazemmi*, Axel Jantsch, Onur Mutlu, Nikil Dutt, **SPECTR: Formal Supervisory Control and Coordination for Many-core Systems Resource Management**, *Proceedings of the Twenty-Third International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*

2018 Bryan Donyanavard, Amir Rahmani, Tiago Mück, Kasra Moazemmi, Nikil Dutt, **Gain Scheduled Control for Nonlinear Power Management in CMPs**, *Design, Automation & Test in Europe Conference & Exhibition (DATE)*

2018 Tiago Mück, Bryan Donyanavard, Kasra Moazemmi, Amir Rahmani, Axel Jantsch, Nikil Dutt, **Design Methodology for Responsive and Robust MIMO Control of Heterogeneous Multicores**, *IEEE Transactions on Multi-Scale Computing Systems (TMSCS)*

2018 Majid Shoushtari, Bryan Donyanavard, Luis Angel D Bathen, Nikil Dutt, **ShaVe-ICE: Sharing Distributed Virtualized SPMs in Many-Core Embedded Systems**, *ACM Transactions on Embedded Computing Systems (TECS)*

2017 Tiago Mück, Bryan Donyanavard, Nikil Dutt, **PoliCym: Rapid Prototyping of Resource Management Policies for HMPs**, *Proceedings of the 28th International Symposium on Rapid System Prototyping: Shortening the Path from Specification to Prototype (RSP)*

2016 Aviral Shrivastava, Nikil Dutt, Jian Cai, Majid Shoushtari, Bryan Donyanavard, Hossein Tajik, **Automatic Management of Software Programmable Memories in Many-core Architectures**, *IET Computers & Digital Techniques*

2016 Bryan Donyanavard, Tiago Mück, Santanu Sarma, Nikil Dutt, **SPARTA: Runtime Task Allocation for Energy Efficient Heterogeneous Many-cores**, *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*

2016 Hossein Tajik, Bryan Donyanavard, Nikil Dutt, **On Detecting and Using Memory Phases in Multimedia Systems**, *Proceedings of the 14th ACM/IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia)*

2016 Hossein Tajik, Bryan Donyanavard, Janmartin Jahn, Joerg Henkel, Nikil Dutt, **SPMPool: Runtime SPM Management for Memory-Intensive Applications in Embedded Many-Cores**, *ACM Transactions on Embedded Computing Systems (TECS)*

2010 Yi-Chu Wang, Bryan Donyanavard, Tim Cheng, **Energy-Aware Real-Time Face Recognition System on Mobile CPU-GPU Platform**, *European Conference on Computer Vision (ECCV Workshops)*

Selected Projects

OS/middleware	Contributed to MARS resource management policy framework and offline simulator - `https://github.com/duttresearchgroup/MARS`
gem5	Added support for software programmable memories (SPMs) in gem5 - `https://github.com/duttresearchgroup/gem5-spm`
LLVM	Implemented basic loop permutation for C Programs in LLVM - Winter 2014
Android	Designed and created a general purpose geo-location application that utilized location information, wireless communication, and Google API to provide multiple functions in Android - Winter 2010
DFT	Implemented full and partial scan and generated high quality test sets for multiple fault models for a RISC8 - 16C57 compatible processor using DFTAdvisor, FastScan, FlexTest - Winter 2009
Behavioral HDL	Implemented superscalar instruction dispatch unit for Tomasulo Algorithm in Verilog RTL - Winter 2009
Behavioral HDL	Implemented a multi-level, multi-processor coherent cache memory design including cache coherency and replacement protocols for a set-associative cache memory in Verilog - Spring 2010
FPGA	Designed and implemented a scalable interconnection network and communication protocol in HDL for Xilinx PicoBlaze microcontrollers on a Xilinx Spartan3E FPGA - Fall 2009

Academic Services

Peer Reviewer	CASES 2014, ESTIMedia 2014, ACM SAC 2014+2016, ACM TODAES 2015, CODES+ISSS 2015–2016, VLSI Design 2016–2017, SCOPES 2016, DATE 2017–2019, GLSVLSI 2018–2019, IEEE TC 2018, ACM TACO 2018, IEEE TVLSI 2019 ($\times$2)

References

Nikil Dutt
Chancellor's Professor
Department of Computer Science
University of California, Irvine
Irvine, CA 92697-3435
✉ dutt@ics.uci.edu
☎ +1.949.824.7219

Andreas Herkersdorf
Professor, Head of the Chair of Integrated Systems
Technische Universität München
Arcisstraße 21
80290 München
✉ herkersdorf@tum.de
☎ +49.89.289.22515

Fadi Kurdahi
Professor, Director of CECS
The Henry Samueli School of Engineering
University of California, Irvine
Irvine, CA 92697-2625
✉ kurdahi@uci.edu
☎ +1.949.824.8104

Amir M. Rahmani
Marie Curie Global Fellow, Docent
Institute for Computer Technology
TU Wien
Gußhausstr. 27-29
1040 Wien, Austria
✉ amirr1@uci.edu
☎ +1.213.716.9248