Nodari Sitchinava

Curriculum Vitae

University of Hawaii, Manoa
Department of Information and Computer Sciences
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Education

2009 Ph.D. (Computer Science), *University of California, Irvine*
Thesis: "Parallel external memory model and algorithms for multicore architectures"
Advisor: Michael T. Goodrich

2003 M.Eng. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*
Thesis: "Dynamic scan chains – a novel architecture to lower the cost of VLSI test"
Advisors: Rohit Kapur and Daniel A. Spielman

2002 S.B. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*

Professional Experience

University of Hawaii, Manoa — Honolulu, HI
Assistant Professor — Jan. 2014 – present

Karlsruhe Institute of Technology — Karlsruhe, GERMANY
Postdoctoral Researcher (Host: Prof. Peter Sanders) — Sept. 2011 – Dec. 2013

MADALGO, University of Aarhus — Aarhus, DENMARK
Postdoctoral Researcher (Host: Prof. Lars Arge) — Sept. 2009 – Sept. 2011

Synopsys, Inc. — Mountain View, CA
Research & Development Engineer in VLSI Test R&D Group — Sept. 2003 – Sept. 2004

Research Interests

Computational models for multicores and GPUs, parallel external memory and cache-oblivious algorithms, parallel data structures, energy-efficient computation, distributed processing of massive data

Teaching Experience

1. Lectures and Seminars

Lecturer, University of Hawaii, Manoa — Spring 2014
Undergraduate course "ICS 491: Parallel Algorithms".

Lecturer, Karlsruhe Institute of Technology — Winter 2012/2013
Graduate course "Algorithms for memory hierarchies".

Lecturer, Karlsruhe Institute of Technology — Summer 2012
Seminar "Algorithms for realistic parallel models".

Co-Lecturer, MADALGO, University of Aarhus — Spring 2010
Graduate course "I/O-efficient graph algorithms". Together with Prof. Norbert Zeh and Dr. Deepak Ajwani.

Co-Lecturer, MADALGO, University of Aarhus Summer 2008
Summer school on cache-oblivious algorithms. Together with Professors Gerth Stølting Brodal, Erik Demaine and Norbert Zeh. Attended by 60 faculty, graduate students and post-docs.

2. Invited Lectures

Guest Lecturer, Karlsruhe Institute of Technology Winter 2011/2012
"Algorithms II" by Prof. Peter Sanders.

Guest Lecturer, Karlsruhe Institute of Technology Winter 2011/2012
"Algorithms engineering" by Prof. Peter Sanders.

Guest Lecturer, MADALGO, Aarhus University Spring 2011
Graduate course "I/O algorithms" by Prof. Lars Arge.

Guest Lecturer, UC Irvine Spring 2008
Graduate course ICS 261 "Data structures" by Prof. David Eppstein.

Publications (alphabetical author order, except when marked with *)

1. Refereed Conference Publications

[C-1] R. Jakob, T. Lieber, N. Sitchinava. On the complexity of list ranking in the parallel external memory model, in *Proceedings of the 39th International Symposium on Mathematical Foundations of Computer Science (MFCS)*, 2014, to appear.

[C-2] P. Afshani, N. Sitchinava. I/O-efficient range minima queries. In *Proceedings of the 14th Scandinavian Symposium and Workshops on Algorithm Theorty (SWAT)*, pages 1-12, 2014.

[C-3] D. Ajwani, N. Sitchinava. Empirical evaluation of the parallel distribution sweeping framework on multicore architectures. In *Proceedings of the 21st European Symposium on Algorithms (ESA)*, pages 25-36, 2013.

[C-4] M. Birn, V. Osipov, P. Sanders, C. Schulz, N. Sitchinava. Efficient parallel and external matching. In *Proceedings of the 19th International Conference Euro-Par 2013 Parallel Processing (Euro-Par)*, pages 659-670, 2013.

[C-5] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. In *Proceedings of the 13th International Symposium on Algorithms and Data Structures (WADS)*, pages 37-48, 2013.

[C-6] N. Sitchinava, N. Zeh. A parallel buffer tree. In *Proceedings of the 24th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 214-223, 2012.

[C-7] M.T. Goodrich, N. Sitchinava, Q. Zhang. Sorting, searching and simulation in the MapReduce framework. In *Proceedings of the 22nd International Symposium on Algorithms and Computation (ISAAC)*, pages 374-383, 2011.

[C-8] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. In *Proceedings of the 26th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1114-1123, 2011.

[C-9] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. In *Proceedings of the 18th European Symposium on Algorithms (ESA)*, pages 75-86, 2010.

[C-10] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory graph algorithms. In *Proceedings of the 25th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1-11, 2010.

[C-11] L. Arge, M.T. Goodrich, M. Nelson, N. Sitchinava. Fundamental parallel algorithms for private-cache chip multiprocessors. In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 197-206, 2008.

[C-12] D. Eppstein, M.T. Goodrich, N. Sitchinava. Guard placement for efficient point-in-polygon proofs. In *Proceedings of the 23rd Annual ACM Symposium on Computational Geometry (SoCG)*, pages 27-36, 2007.

[C-13] * N. Sitchinava, S. Samaranayake, R. Kapur, E. Gizdarski, F. Neuveux, T.W. Williams. Changing scan enable during shift. In *Proceedings of the 22nd IEEE VLSI Test Symposium (VTS)*, pages 73-78, 2004.

[C-14] * S. Samaranayake, E. Gizdarski, N. Sitchinava, F. Neuveux, R. Kapur, T.W. Williams. A reconfigurable shared scan-in architecture. In *Proceedings of the 21st IEEE VLSI Test Symposium (VTS)*, pages 9-14, 2003.

2. Journal Publications

[J-1] N. Sitchinava. Computational geometry in the parallel external memory model. SIGSPATIAL Special 4(2): 18-23 (2012).

[J-2] * S. Samaranayake, N. Sitchinava, R. Kapur, M. Amin, T.W. Williams. Dynamic Scan: driving down the cost of test. IEEE Computer 35(10): 63-68 (2002).

3. Patents

[P-1] * R. Kapur, N. Sitchinava, S. Samaranayake, E. Gizdarski, F. Neuveux, S. Duggirala, T.W. Williams. Dynamically reconfigurable shared scan-in test architecture. US Patents 7900105, 7836368, 7836367, 7774663, 7743299, 7596733, 7418640.

4. Refereed Workshop Presentations

[W-1] N. Sitchinava, V. Weichert. Provably-efficient GPU algorithms. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2013.

[W-2] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2013.

[W-3] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2011.

[W-4] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2010.

[W-5] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory model. *Workshop on Theory and Many-Cores (T&MC)*, 2009.

[W-6] * N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams. Dynamically reconfigurable shared scan-in architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2004.

[W-7] * N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams, D. Spielman. A segment identification algorithms for a dynamic scan architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2003.

[W-8] * N. Sitchinava, S. Samaranayake, R. Kapur, M. Amin, T.W. Williams. DFT – ATE solution to lower the cost of test. *IEEE Workshop on Test Resource Partitioning*, 2001.

Conference and Workshop Keynote Talks

"Data locality in high-performance computing", Workshop on Scientific Computing Carpentry, 2013

Selected Invited Talks

University of Chile (Host: Prof. Jérémy Barbay) October 27, 2013
Title: "(Dynamic) RMQ in the External Memory and Cache-oblivious models"

Georgetown University (Host: Prof. Jeremy T. Fineman) November 14, 2013
Title: "Locality-conscious parallel algorithms"

Stony Brook University (Host: Prof. Michael A. Bender) November 13, 2013
Title: "Locality-conscious parallel algorithms"

University of Patras (Host: Prof. Christos D. Zaroliagis) October 22, 2013
Title: "PEM model and its application to GPU computing"

University of Ljubljana (Host: Prof. Andrej Brodnik) October 17, 2013
Title: "Locality-conscious parallel algorithms"

ETH Zurich (Host: Dr. Riko Jacob) October 14, 2013
Title: "Parallel External Memory (PEM) model and its application to GPU computing"

University of Kansas (Host: Prof. Joseph Evans) April 8, 2013
Title: "Data locality in high-performance computing"

TU Eindhoven (Host: Prof. Mark de Berg) May 4, 2012
Title: "A parallel buffer tree"

Georgia Institute of Technology (Host: Prof. David Bader) March 17, 2011
Title: "Parallel computing – a theoretical perspective"

Goethe University Frankfurt (Host: Prof. Dr. Ulrich Meyer) December 20, 2010
Title: "Parallel computing – a theoretical perspective"

University of California, Irvine (Host: Prof. Michael Goodrich) April 30, 2010
Title: "Geometric algorithms for private-cache chip multiprocessors"

Cambridge University (Host: Prof. Simon Moore) April 22, 2009
Title: "Parallel external memory model for multicore architectures"

Dalhousie University (Host: Prof. Norbert Zeh) October 16, 2008
Title: "Parallel external memory model for multicore architectures"

Leadership and Professional Service

Program Committee Service:

- ◇ *Chair*, Sixth Workshop on Massive Data Algorithmics (MASSIVE), 2014
- ◇ 26th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2014
- ◇ Meeting on Algorithm Engineering & Experiments (ALENEX), 2014
- ◇ Fifth Workshop on Massive Data Algorithmics (MASSIVE), 2013

External Reviewer (Journals):

- ◇ Journal of the ACM (JACM)
- ◇ Algorithmica
- ◇ International Journal of Computational Geometry and Applications (IJCGA)
- ◇ IEEE Transactions on Parallel and Distributed Systems (TPDS)
- ◇ Parallel Computing
- ◇ Computational Geometry: Theory and Applications (CGTA)

External Reviewer (Conferences):

- ◇ ACM-SIAM Symposium on Discrete Algorithms (SODA)

- ◇ International Colloquium on Automata, Languages, and Programming (ICALP)
- ◇ Europeans Symposium on Algorithms (ESA)
- ◇ ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)
- ◇ IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- ◇ International Symposium on Algorithms and Computation (ISAAC)
- ◇ ACM SIGSPATIAL International Conference on Advances in Geographic Information Systems (ACM SIGSPATIAL GIS)
- ◇ Symposium on Experimental Algorithms (SEA)
- ◇ Latin American Theoretical Informatics Symposium (LATIN)
- ◇ International Conference Euro-Par Parallel Processing (Euro-Par)