

ICS 121 Lecture Notes

Topic 10
Formal Methods ¹

What are Formal Methods?

ICS 121

- **Formal Method (FM) =**
specification language + formal reasoning
- **Body of techniques supported by**
 - precise mathematics
 - powerful analysis tools
- **Rigorous effective mechanisms for system**
 - modeling
 - synthesis
 - analysis

```
graph LR; modeling --> Specification; Specification -- synthesis --> Implementation; Implementation -- analysis --> Specification;
```

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What are Formal Methods?

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- **Use of formalisms**
 - e.g., logic, discrete mathematics, finite state machines
- **In system descriptions**
 - e.g., system models, constraints, specifications, designs
- **For broad range of effects**
 - e.g., highly reliable, secure, safe systems and more effective production
- **And varying levels of use**
 - *guidance*: structuring what to say
 - *documentation*: unambiguous communication
 - *rigor*: formal specification and proofs
 - *mechanisms*: proof assistance, testing

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Formal Specification in Software Development

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- **Formal specifications ground the software development process in the well-defined basis of computer science**
- **Emphasis switches from customer to developer**
- **Formal specification expressed in language whose syntax and semantics are formally defined**
 - hierarchical decomposition
 - mathematical foundation
 - graphical presentation
 - accompanied by informal description

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Goals and Objectives

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- **Requirements Specification**
 - clarify customer's requirements
 - reveal ambiguity, inconsistency, incompleteness
- **System/Software Design**
 - decomposition structural specifications of component relations and behavioral specification of components
 - refinement demonstrating that next level of abstraction satisfies higher level
- **Verification**
 - proving a specificand (implementation) satisfies its specification
- **Validation**
 - testing and debugging
- **Documentation**
 - communication between specifier, implementor, customer, clients

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Specification and Design

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```
graph LR; A[Requirements-Analysis and Definition] --> B[Requirements-Specification]; B --> C[Design];
```

Increasing contractor involvement
Decreasing client involvement

SPECIFICATION

DESIGN

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Benefits of Using Formal Specifications and Methods

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- higher quality software
- verifiability of implementation
- insight and understanding
- minimized maintenance and cost
- automated assistance
- simulation, animation, execution
- formal analysis
- guidance for testing
- transformation technology
- reduced liability and risks
- standard satisfaction

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Formal Specifications are not yet widely used

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- **Reasons**
 - emerging technology with unclear payoff
 - little experience
 - lack of automated support
 - not especially user friendly
 - too many in-place techniques and tools
- **Excuses**
 - high learning curve
 - mathematical sophistication required
 - techniques not widely applicable
 - ignorance of advances

Formal Specification Languages

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- **A formal specification language consists of**
 - *syntax* (the notation)
 - *semantics* (the meaning)
 - *satisfies* (relation defining which objects satisfy which notations)
- **A formal specification defines**
 - *syntax* (signature of the mapping)
 - *semantics* (meaning of the mapping)
 - *exceptions* (undefined/erroneous mappings)
- **If sat(syn,sem) then**
 - syn is a *specification* of sem
 - sem is a *specificand* of syn

Desirable Properties

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- **Consistency**
 - a specificand exists that satisfies a specification
- **Completeness (incrementally)**
 - all aspects of specificands are specified
- **Unambiguous**
 - exactly one specificand satisfies a specification (may be a set if specification is not complete)
- **Inference**
 - consequence relation used to prove properties about the specificands that satisfy a specification

Types of Formal Specifications

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- **Behavioral specifications describe constraints on behavior of specificand – e.g.,**
 - functionality
 - safety
 - security
 - performance
- **Structural specifications describe constraints on internal composition of specificand**
 - module interconnection
 - uses and *is-composed-of*
 - dependence relations

Characteristics

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- **Model-oriented Specifications**
 - specify system behavior by constructing a model in terms of well-defined mathematical constructs
- **Property-oriented Specifications**
 - specify system behavior in terms of properties that must be satisfied
- **Visual Specifications**
 - specify system behavior and structure by graphical depictions
- **Executable Specifications**
 - specify system behavior completely enough that specifications can run on a computer
- **Tool Support**
 - syntactic checking
 - model checking
 - proof checking

Basic Specification Language Types

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- **Abstract Model Specifications**
 - defines operations in terms of well-defined mathematical model
- **Algebraic Specifications**
 - defines operations by a collection of equivalence relations
- **State Transition Specifications**
 - defines operations in terms of states and transitions
- **Axiomatic Specifications**
 - defines operations by logical assertions

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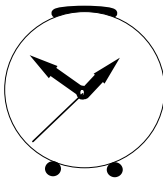
Formal Specification Languages: Clock Example

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- Initially, the time is midnight, the bell is off, and the alarm is disabled.
- Whenever the current time is the same as the alarm time and the alarm is enabled, the bell starts ringing.

This is the only condition under which the bell begins to ring.

- The alarm time can be set at any time.
- Only when the alarm is enabled can it be disabled.
- If the alarm is disabled while the bell is ringing, the bell stops ringing.
- Resetting the clock and enabling or disabling the alarm are considered to be done instantaneously.



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1 Abstract Model Specifications

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- Explicitly describes behavior in terms of a model using well-defined types (sets, sequences, relations, functions) and defines operations by showing effects on model
- Specification includes
 - type: syntax of object being specified
 - model: underlying structure
 - invariant: properties of modeled object
 - pre/post conditions: semantics of operations
- Pros and Cons
 - state is made explicit in model
 - suggests an implementation
 - widely applicable because of modeling orientation
- Various notations: VDM, Z, RAISE

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Abstract Model Specifications

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- Objects specified by effect of operations on a model in terms of well-understood mathematical entities (e.g., sets, sequences, relations, functions)
- State is explicit in the model
- Objects can be built hierarchically
- Specification using Z abstract model specifications
 1. establish the object schemas (objects and attributes)
 - including invariant properties of objects
 2. establish the operation schemas
 - schema modifiability (E vs. E schema)
 - operation signatures (input? vs. output!)
 - state modifications (attribute vs. attribute')

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Abstract Model Specifications: the Z Notation

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specification name [generic parameters]

signature

predicate

- a Z specification is a collection of schemas
- a **schema** introduces some entities and invariant properties
- the signature may make a defined schema visible
- the schema signature defines each entity's name and type (syntax)
- the **predicate** defines the relationships between the entities that must always hold (semantics)
- should be supported by informal description

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Abstract Model Specifications: Z Clock - 1

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BellStatus: {quiet, ringing}, AlarmStatus: {disabled, enabled}

Clock
 time, alarm_time: N
 bell: BellStatus
 alarm: AlarmStatus

InitClock
 Δ Clock
 $(time' = midnight) \wedge (bell' = quiet) \wedge (alarm' = disabled)$

Tick
 Δ Clock
 $(time' = succ(time))$
 $(alarm_time' = time') \wedge (alarm' = enabled) \Rightarrow (bell' = ringing)$
 $(\neg(alarm_time' = time') \wedge (alarm' = enabled)) \Rightarrow (bell' = bell)$
 $(alarm' = alarm) \wedge (alarm_time' = alarm_time)$

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Abstract Model Specifications: Z Clock - 2

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SetAlarmTime
 Δ Clock
 new_time?: N
 $(alarm_time' = new_time?)$
 $((alarm_time' = time') \wedge (alarm' = enabled) \Rightarrow (bell' = ringing))$
 $(\neg(alarm_time' = time') \wedge (alarm' = enabled)) \Rightarrow (bell' = bell)$
 $(time' = time) \wedge (alarm' = alarm)$

EnableAlarm
 Δ Clock
 $(alarm = disabled) \Rightarrow (alarm' = enabled) \wedge$
 $((alarm_time' = time') \Rightarrow (bell' = ringing) \wedge$
 $(\neg(alarm_time' = time') \Rightarrow (bell' = bell)) \wedge$
 $(time' = time) \wedge (alarm_time' = alarm_time)$

DisableAlarm
 Δ Clock
 $(alarm = enabled) \Rightarrow (alarm' = disabled) \wedge (bell' = quiet) \wedge$
 $(time' = time) \wedge (alarm' = alarm) \wedge (alarm_time' = alarm_time)$

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Algebraic Specification

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- Objects specified as algebraic sorts in terms of equivalence relations between associated operations
- State is concealed in objects
- Objects can be built hierarchically
- Specification using algebraic sorts
 1. establish the sorts (objects and attributes)
 2. establish the necessary operations
 - constructor operations
 - access operations
 3. establish the equivalence relations
 - rule of thumb: a relation for each access over each constructor
 - simplified when constructors defined in terms of imports

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Algebraic Specifications - 2

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- Specification includes
 - functionality: syntax and legal constructions
 - relations: semantics by equivalence classes
- Pros and Cons
 - only pure functions described (no side effects)
 - supports extensibility of data abstractions
 - often hard to comprehend and construct
 - particularly applicable to abstract data types
- Various notations: OBJ, Larch, Clear, Anna

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Algebraic Specifications: a simple notation

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specification name (generic parameters)
sort name
imports list of specification names
operation signatures
relations

- an algebraic specification is a collection of sorts
- a **sort** specifies an object class (or abstract data type)
- **importing** specifications makes their defined sorts visible
- the **operation signatures** define each operation's name and the sorts of parameters and results (syntax)
- the **relations** define the effect of applying operations (semantics)
- should be supported by informal description

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Algebraic Specifications: Algebraic CLOCK

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operation signatures

init: \rightarrow CLOCK

tick: CLOCK \rightarrow CLOCK

setalarm: CLOCK x TIME \rightarrow CLOCK

enable: CLOCK \rightarrow CLOCK

disable: CLOCK \rightarrow CLOCK

time: CLOCK \rightarrow TIME

alarm_time: CLOCK \rightarrow TIME

bell: CLOCK \rightarrow {ringing, quiet}

alarm: CLOCK \rightarrow {on, off}

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Algebraic Specifications: Algebraic CLOCK - 2

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relations

time(init) \rightarrow midnight

time(tick(C)) \rightarrow time(C) + 1

time(setalarm(C,T)) \rightarrow time(C)

time(enable(C)) \rightarrow time(C)

time(disable(C)) \rightarrow time(C)

alarm_time(init) \rightarrow midnight

alarm_time(tick(C)) \rightarrow alarm_time(C)

alarm_time(setalarm(C,T)) \rightarrow T

alarm_time(enable(C)) \rightarrow alarm_time(C)

alarm_time(disable(C)) \rightarrow alarm_time(C)

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Algebraic Specifications: Algebraic CLOCK - 3

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bell(init) \rightarrow quiet

bell(tick(C)) \rightarrow (if alarm_time(tick(C)) = time(tick(C)) and alarm(C) = on then ringing else quiet)

bell(setalarm(C,T)) \rightarrow (if T = time(C) and alarm(C) = on then ringing else quiet)

bell(enable(C)) \rightarrow (if alarm_time(C) = time(tick(C)) then ringing else quiet)

bell(disable(C)) \rightarrow quiet

alarm(init) \rightarrow off

alarm(tick(C)) \rightarrow alarm(C)

alarm(setalarm(C,T)) \rightarrow alarm(C)

alarm(enable(C)) \rightarrow (if alarm(C) = off then on)

alarm(disable(C)) \rightarrow (if alarm(C) = on then off)

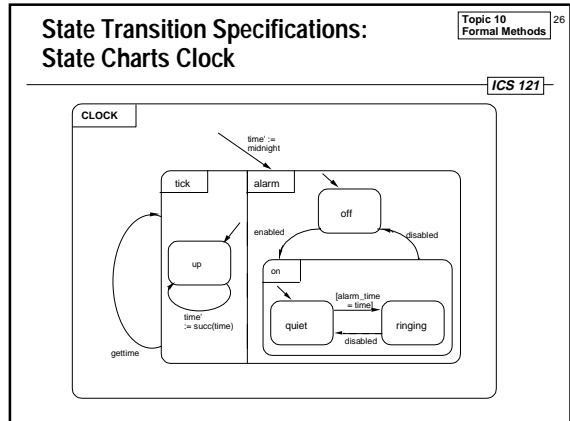
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③ State Transition Specifications

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- **Explicitly describes system behavior by a set of states and defines operations as transitions between states or observations on state**
- **Specification includes**
 - states: possible values
 - transitions: semantics by state transformations and observations
- **Pros and Cons**
 - free of representational details (except augmentations)
 - state explosion is common
 - extensions to minimize states and modularize
 - particularly applicable to control systems, languages, hardware
- **Graphical as well as textual notations: StateCharts, ASLAN, Paisley, InaJo, Special**



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State Transition Specifications: ASLAN Clock

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SPECIFICATION Clock

LEVEL Top_Level

TYPE BellStatus IS (quiet, ringing), AlarmStatus IS (disabled, enabled)

VARIABLE time, alarm_time: INTEGER, bell: BellStatus, alarm: AlarmStatus

INITIAL (time = midnight) & (bell = quiet) & (alarm = disabled)

INVARIANT TRUE

TRANSITION tick

ENTRY TRUE

EXIT (time = succ(time'))
& (if ((alarm_time = time) & (alarm = enabled))
then (bell = ringing) else (bell = bell') fi)
& (alarm = alarm') & (alarm_time = alarm_time')

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State Transition Specifications: ASLAN Clock - 2

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TRANSITION set_alarm (new_time: INTEGER)

ENTRY TRUE

EXIT (alarm_time = new_time)
& (if ((alarm_time = time) & (alarm = enabled))
then (bell = ringing) else (bell = bell') fi)
& (time = time') & (alarm = alarm')

TRANSITION enable_alarm

ENTRY alarm = disabled

EXIT (alarm = enabled)
& (if (alarm_time = time)
then (bell = ringing) else (bell = bell') fi)
& (time = time') & (alarm_time = alarm_time')

TRANSITION disable_alarm

ENTRY alarm = enabled

EXIT (alarm = disabled) & (bell = quiet)

END Top_Level

END Clock

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④ Axiomatic Specifications

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- **Implicitly defines behavior in terms of [first-order] logic formulas specifying input/output assertions (and possibly intermediate assertions)**
- **Specification includes**
 - operation interfaces: input/output parameters
 - operation axioms: pre/post assertions on input/output
- **Pros and Cons**
 - fairly easy to understand
 - widely applicable (although hard to scale up)
 - most widely used technique in proving (inductive assertion method)
 - foundation of mathematics in software development
- **Many languages support this type of specification:**
 - VDM, Anna
 - Extensions include various logics for specific application domains (e.g., temporal logic: RTIL, GIL)

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Axiomatic Specifications: VDM Clock

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INIT()

ext wr time: N, bell: {quiet, ringing}, alarm: {disabled, enabled}

pre true

post (time' = midnight) ∧ (bell' = quiet) ∧ (alarm' = disabled)

TICK()

ext wr time: N, bell: {quiet, ringing}

rd alarm_time: N, alarm: {disabled, enabled}

pre true

post (time' = succ(time)) ∧ (if (alarm_time' = time') ∧ (alarm' = enabled)
then (bell' = ringing) else (bell' = bell))

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Axiomatic Specifications: VDM Clock - 2

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SETALARMTIME(new_time: N)
ext wr alarm_time: N, bell: {quiet, ringing}
rd time: N, alarm: {disabled, enabled}
pre true
post (alarm_time' = new_time) \wedge (if (alarm_time' = time') \wedge (alarm' = enabled)
then (bell' = ringing) else (bell' = bell))

ENABLEALARM()
ext wr alarm: {disabled, enabled}, bell: {quiet, ringing}
rd time: N, alarm_time: N
pre alarm = disabled
post (alarm' = enabled) \wedge (if (alarm_time' = time')
then (bell' = ringing) else (bell' = bell))

DISABLEALARM()
ext wr alarm: {disabled, enabled}, bell: {quiet, ringing}
pre alarm = enabled
post (alarm' = disabled) \wedge (bell' = quiet)