Short Postmortem

• Some worked on the old version of the code with 8 PEs.
  • Evaluation was done after adjusting performance to 16 PEs.

• With 16 PEs, Maximum Op/Cycle is 16
  • Can we achieve this? Why or why not?

• Clock speed is restricted by critical path. Critical path sources:
  • Old code: Use of partialSumIdxQ2
  • New code: SDRAM controller
  • Both are around 60 to 70 MHz
Derby Results

Ops/Cycle rarely reaches 4! Why not 16?
Ops/Cycle, why not 16?

- If done well, computation is not bottleneck
  - 16 PEs, should be able to reach 16

- Weight memory access is not bottleneck
  - Some of you have noticed performance scaling ends even with more weight replication

- Is the bottleneck getting the input data?
  - Yes! Uart module emits data at maximum 8 bits/cycle
    - And this is in simulation! Physical Uart has much lower baud rate due to baud rates
  - At least 4 cycles per Float!
  - Does this matter? Perhaps, maybe if input itself is slow, we don’t need all these PEs... Depends on the application!